Numerical Calibration and De-embedding Techniques for CAD and Equivalent Circuit Models of Electromagnetic Structures

Ke Wu, Lin Li

Abstract **--- The numerical calibration and de-embedding techniques used in the planar electromagnetic (EM) simulation are reviewed. These techniques are used to eliminate the port discontinuities brought by the current/voltage exciting source. Therefore, accurate equivalent circuit model of the planar discontinuities can be extracted.**

Index Terms **– calibration technique, equivalent circuit model, planar discontinuity and circuit, full-wave electromagnetic simulation.**

I. INTRODUCTION

The state-of-the-art design of planar microwave and millimeter-wave circuits and components is generally made in two different ways. One is based on lumped-element network topologies, which are developed with static or quasi-static equivalent circuit models of electrically small-sized structures or discontinuities and connecting transmission lines such as planar microstrip or coplanar waveguide elements. This design procedure is quite similar or identical to the schemes commonly used for low-frequency electronic circuits. A large variety of equivalent circuit models for planar discontinuities has been established and widely used in commercial software packages including Agilent advanced design system (ADS)[1], Agilent EEsof EDA[1], Ansoft designer[2] and others. However, these models and their network parameters are generally formulated by static/quasi-static closed-form equations with approximations or assumptions, which do not account for high frequency effects such as frequency dispersion, high-order modes, parasitic coupling, space radiation and substrate leakage. In addition, a commercial software package may be able to handle only a limited number of all possible planar discontinuities in its design library, and the designer has to develop his/her own models for the other portion of planar discontinuities. Nevertheless, the equivalent network approach is still the most powerful and preferred technique for designer.

The other way is more accurate and reliable that is completely based on full-wave electromagnetic modeling and simulation. The terminology "full-wave" means that the field model is directly developed from the Maxwell's equations although certain assumption or approximation may also be considered in the model construction such as lossless structures and vanishing conductor thickness. A handful of commercial method-of-moments (MoM) simulators including Agilent Momentum, Ansoft Ensemble, Sonnet EM Suite[3], Zeland IE3D[4] and other field-based software packages present popular design tools, allowing one to implement accurate full-wave simulation and optimization of planar integrated circuits and antennas. Generally, the full-wave packages are related to simulation and modeling aspects rather than design and optimization processes even though a sophisticated field-based scheme may be possible at the expense of requiring a huge computational resource. This is in particular true when an electrically large planar structure is designed and optimized. Therefore, the global field-based optimization of such a complete structure is impractical and sometimes impossible with the commonly used computing facility. So the most efficient way is to segment the overall complex geometrical layout into a number of electrically small and geometrically simple discontinuities together with uniform transmission line sections and then carry out a direct synthesis and optimization procedure based on its equivalent circuit network topology, which is constructed by characterization and establishment of equivalent circuit model of each individual part. In this way, element-to-element and adjacent couplings can be involved through multi-level segmentation procedure. However, the fundamental problem in this procedure is whether it is able to obtain very accurate equivalent circuit model with full-wave modeling techniques for such electrically small structures.

The deterministic MOM algorithms [1]–[13] have been recognized as probably the most powerful candidates for accurate and efficient modeling of planar or quasi-planar tructures. However, lumped current/voltage sources such as delta-voltage are generally used to excite the structure, allowing the deterministic and efficient calculations of field parameters. Since the artificial sources can never describe the exact field profile at the ports of excitation because of multilayered geometry and non-uniform field profile, the resulting "artificial" field discontinuities or differences between the lumped sources and the "true" fields can bring errors or parasites to the calculated network parameters or equivalent circuit models, which can be significant for an electrically small structure. To solve this problem of port discontinuities, several techniques were presented [13]-[17]. But no further attempts were published for systematic understanding of this critical problem until the proposal of short-open calibration (SOC) technique [18]-[30].

The SOC technique, which was inspired from the real-world measurement techniques, makes use of the even/odd

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2.Ansoft, 412-261-3200 / Pittsburgh, PA.

3.Sonnet Software, 315-453-3096 / Liverpool, NY.

4.Zeland Software, Inc, 510-623-7162 / Fremont, CA.

excitations with one section of uniform line to formulate the open/short standards and then calculate the error boxes of the structure. Such SOC calibration techniques have successfully been used in equivalent circuit modeling and applications of various microwave planar structures including microstrip, coplanar stripline (CPS), and finite-ground coplanar waveguide (FGCPW) circuits. The original 2-port SOC calibration technique has also been extended to the multi-port SOC [30]. The use of SOC techniques requires intermediate field calculations within the MoM software, which has to be implemented by the software developer. Considering that nearly all commercial MoM simulators can only provide the calculated network parameters at a specified external location along the feeding line, the SOC technique was found difficult in theory for its compatibility and integration with them. Therefore, it is not practical for us to consider the SOC technique in the commercial electromagnetic simulation and analysis. To remove this hurdle, thru-reflect-line (TRL) and thru-resistor (TR) numerical calibration techniques were introduced that have successfully been combined with such commercial EM software packages as Agilent Momentum and Zeland IE3D to model the port discontinuities and extract the circuit model of planar discontinuities[31]-[33] in a similar way as the SOC scheme.

It is well known that the (TRL) calibration technique [34]-[37] has widely been used in microwave measurements and it was also deployed in [17] to numerically extract the S-parameters of planar circuits from full-wave MoM simulations. The TRL standards are easily realized in both practical measurements and numerical simulations. Distinct technical merits of the TRL and TR calibration techniques can be summarized by two aspects, namely, easily realizable calibration standards and complete compatibility with commercial EM software. With the TRL or TR calibration techniques and commercial package, one can easily formulate full-wave based equivalent circuit model of planar circuits. In this paper, these calibration techniques will be described and discussed with respect to their applications. To avoid any possible confusion of terminology in connection with the use of discontinuity, we should point out that the modeling of a planar discontinuity is concerned with the investigation of a "useful" circuit element and its equivalent circuit model will be developed by numerical calibration and parameter extraction while the port discontinuity is related to the parasites due to the "artificial" source or excitation mechanism required in the numerical methods.

II. CALIBRATION TECHNIQUES

In the following, numerical calibration techniques that have developed to date are presented and their technical features are discussed.

A. Double-Delay Calibration

In [15][40], Rautio developed a simple technique called "double-delay calibration" in the MoM algorithm that was used to de-embed port discontinuity effects and compensate calculation errors due to the deterministic source-type formulations. This technique assumes the port discontinuity as a shunt capacitor and uses two line standards to calibrate the error boxes, as shown in Fig. 1. The procedure of the calibration can be summarized as follows:

1. Calculate the ABCD (cascading) matrix for both L and 2L.
2. Invert the 2L-ABCD matrix. This yields the ABCD matrix for a negative 2L length transmission line with inverted port discontinuities on each port.
3. Pre- and post-multiply the inverted 2L-ABCD matrix with the L-ABCD matrix. This leaves the ABCD matrix of the port discontinuity to cascade with itself.
4. To evaluate the port discontinuity by itself, provided that A, B and D are correct, simply divide C by 2.

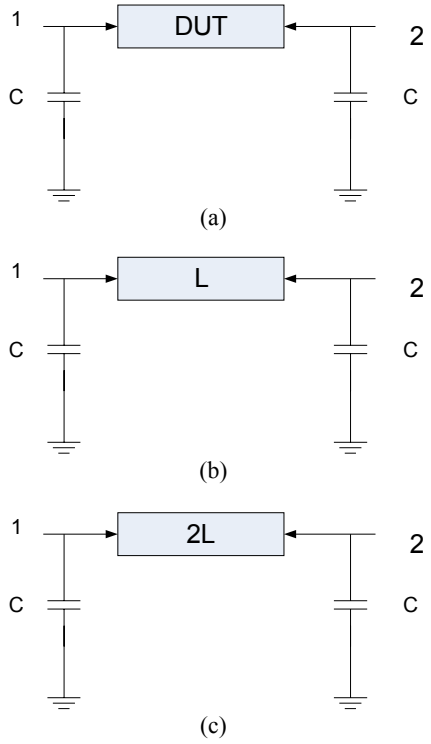

Fig. 1. (a) Port discontinuities (capacitor C) surrounding the device-under-test (DUT); (b) and (c) the two standards required for the electromagnetic de-embedding are a through line of length L and a through line of length 2L. L needs to be only large enough that fringing fields are free from the interaction of the port discontinuities.

B. Soc Calibration

The SOC (short-open calibration) technique was proposed and developed by L. Zhu and K. Wu on the basis of a deterministic MOM algorithm and it has been detailed in [19] for planar circuit modeling problems. The physical structure of a two-port microstrip discontinuity is shown in Fig. 2(a). The corresponding network model of the structure can also be arranged via three distinct circuit topologies, namely, the error box [X_1], the device-under-test (DUT), and the error box [X_2]. They are sequentially cascaded, as shown in Fig. 2(b). In this way, all of the parasitic effects brought by the feed lines and

port discontinuities in the simulation model are considered through network parameters of the two error blocks, which may be considered as "lumped-element" arrangements of the parasitic effects. Fig. 2(c) and (d) show the "short" and "open" circuits (standards) at the reference planes of the feed lines with reference to the two-port unbounded discontinuity of Fig. 2(a). The so-called "short" and "open" elements can actually be formulated by exciting a pair of even and odd impressed voltages (E_{io} and E_{is} for electric fields by equivalence) along a uniform microstrip line, as sketched in Fig 3(a) and (b), whose symmetrical plane T_i becomes open (magnetic wall) and short (electric wall), respectively. To handle the *i*th port block, a uniform microstrip line is suitably selected with a length of twice the distance, which is defined between the port and reference plane of the *i*th feed line, as shown in Fig3(a). Two impressed voltage (or delta voltage) sources are then imposed at the two sides of the uniform line. As such, identical environments for the two-ports are effectively formulated. Obviously, applying "short" and "open" procedures via the impressed voltages or electric fields leads to two sets of equivalent networks, as shown in Fig3(a) and (b), having an idealized open- and short-end, respectively.

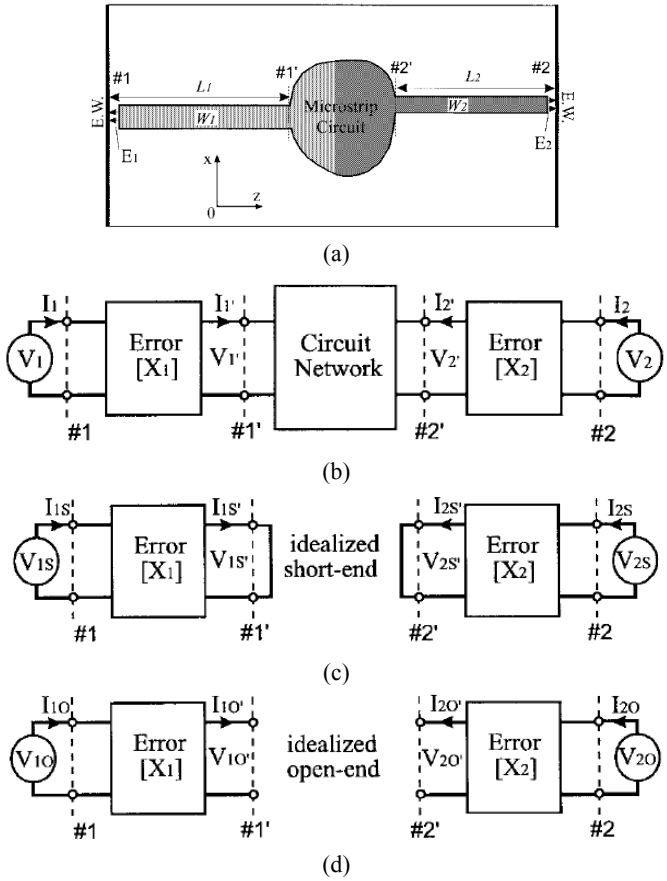

Fig. 2. The network sketch of the SOC technique for a planar circuit. (a) Two-port discontinuity for the MoM modeling; (b) Equivalent network of (a); (c) Short-end circuit element for the SOC model; and (d) Open-end circuit element for the SOC model.

The ABCD matrix of the *i*th error block can be explicitly formulated by equation (1). This equation shows that the ABCD matrix of an error block, accounting for all of the parasitic effects brought by the two non-ideal port discontinuities and two feed lines in the unified dynamic model, can be accurately determined by three terms of numerically "measured" currents: $\overline{I}_{is}$, $\overline{I}_{io}$ and $\overline{I}_{is}'$.

$$X_i = \begin{bmatrix} \overline{I}_{is}/\overline{I}_{is}' & -1/\overline{I}_{is}' \\ -\overline{I}_{is}'\overline{I}_{io}/(\overline{I}_{is}-\overline{I}_{io}) & \overline{I}_{is}'/(\overline{I}_{is}-\overline{I}_{io}) \end{bmatrix} \quad (1)$$

Once the error boxes are calculated, we can easily derive the ABCD matrix of device under test (DUT), $[A_{DUT}]$, with the following equations:

$$[A_{DUT}] = [X_1]^{-1}[A_{EXT}][X_2]^{-1} \quad (2)$$

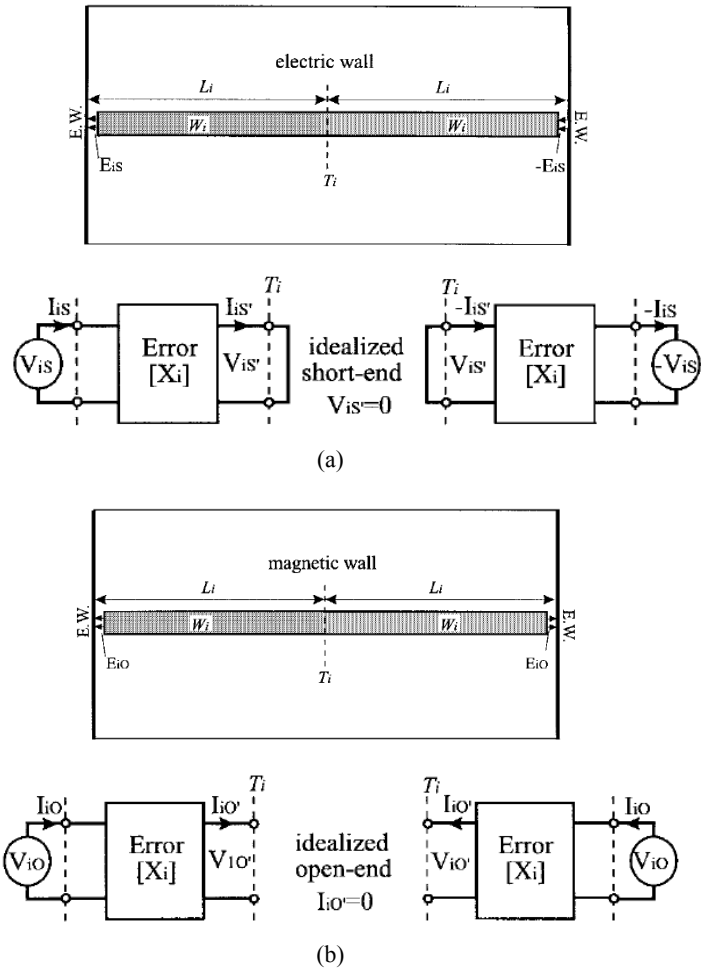

Fig. 3. Physical models and circuit networks of the ideal "open" and "short" line elements realized by a pair of even- and odd-oriented electric-field excitations for the 3-D MoM algorithm. (a) Ideal "short" line element and its circuit model; and (b) Ideal "open" line element and its circuit model.

Extensive investigations and many examples have been presented in various SOC-related publications. One example of a microstrip open-end deposited on an electrically thin dielectric substrate was studied to show the application of the SOC in the circuit model's parameter extraction.

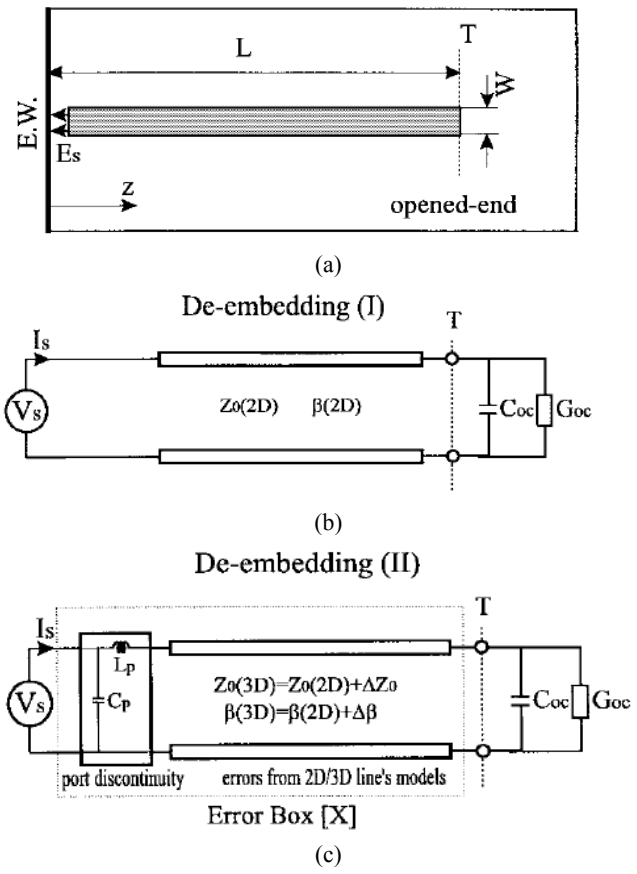

Fig. 4. A generalized unbounded microstrip open-end circuit framework and its equivalent circuit model. (a) Physical layout; (b) Conventional de-embedding procedure (De-embedding I); and (c) SOC technique (De-embedding II).

For comparison, two de-embedding techniques, called De embedding (I), depicted in Fig. 4(b), and De-embedding (II), depicted in Fig. 4(c) were simultaneously used to extract the equivalent parasitic capacitance for the open-endThe results for the normalized capacitance are plotted in Fig. 5 with the results simulated by a static model [38]. It shows that the De-embedding (I) yields an oscillatory curve for the capacitance versus the line length so that it is not reliable or not correct. This is because the model was developed on the basis of a physical approximation that ignores the parasitic effect brought by a non-ideal excitation model and also the resulting consistency problem of the 2-D and 3-D algorithms, for example, 2-D and 3-D impedance definitions.

The port discontinuity introduced at the source plane using the impressed voltage excitation is modeled as an equivalent circuit network through the application of the SOC technique [20].The circuit network can be an purely shunt capacitor and a series impedance below 6 GHz, as shown in Fig. 6. Such low-frequency results suggest that the assumption used in the above-discussed "double-delay calibration" is valid only for a low-frequency range.

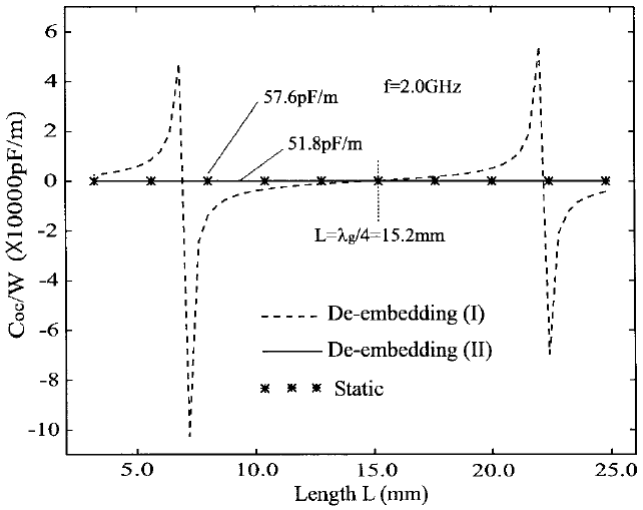

Fig. 5. Simulated open-end capacitance Coc of an open-ended line using the impressed-voltage-source MoM algorithm for a different line length L that is defined between the port and open-end location. (w = h = 0.635mm, εr = 9.9)

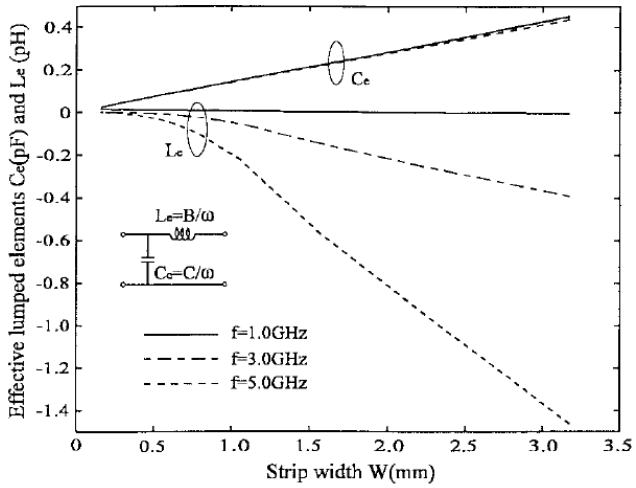

Fig. 6. Electrical behaviors of the equivalent shunt capacitance Ce and series inductance Le as a function of the strip width at low frequency.

C. TRL Calibration

Similar to the real measurement, the proposed numerical TRL calibration [31] by the authors uses three standards: thru, reflect and line connections. Unlike the SOC calibration, the TRL calibration doesn't need to measure (or calculate) the current/voltage at the reference planes of the device under test. In addition, any additional simulation of current density distributions along the feeding line is not required in the indirect MoM algorithm as in the SOC technique. Therefore, this technique is designed for its direct compatibility with commercial software packages. The TRL calibration procedure can be illustrated as in Fig. 7. At first, the S-matrix parameters at the two external ports can easily be obtained by using numerical simulations with a commercial MoM simulator. In [31], the IE3D package of Zeland Inc was used. Then such S-matrix is converted into its corresponding wave cascading matrix [T].

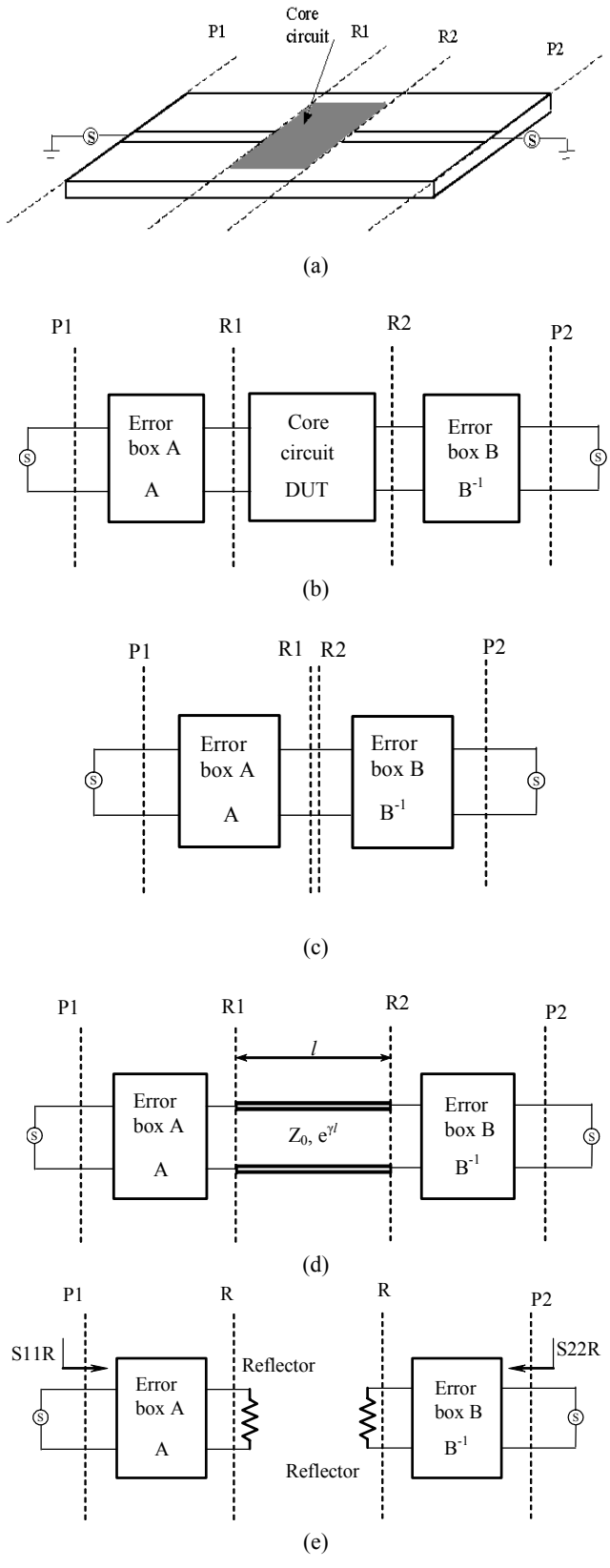

Fig. 7. Block diagrams of the numerical TRL calibration procedure. (a) Two-port core circuit under modeling. (b) Error model for numerical TRL calibration. (c) Through standard connection. (d) Line standard connection. (e) Reflect standard connection.

In Fig. 7(b), the terms $[T_A]$, $[T_B]$ and $[T_{DUT}]$ stand for the wave cascading matrices of two error boxes and DUT box, respectively. In order to evaluate and calibrate out these two error boxes, three TRL calibration standards, i.e., thru, reflect and line connections, are defined in the format of equivalent network topology as shown in Fig. 7(c-e). With the same definition as in [34][35], one can define

$$M_x = AN_xB^{-1} \tag{3}$$

in which A and B^{-1} is the cascading matrices of the error box A and B; N_x is the cascading matrices of the standards and M_x is the cascading matrices obtained at reference planes P_1 and P_2.

For the through standard and the line standard, we have

$$N_1 = \begin{bmatrix} I & 0 \\ 0 & I \end{bmatrix} \tag{4}$$

$$N_2 = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix} \tag{5}$$

As stated in [34][35], error parameters in the error box can be determined by measurements of the three TRL standards connections and the true parameters of the DUT can be extracted correctly. As in [35], we define two similar matrices P and Q as follows

$$Q = M_2M_1^{-1} \text{ and } P = N_2N_1^{-1} \text{ with } P = A^{-1}QA \tag{6}$$

Because P and Q are similar, we can define an eigenvalue matrix Λ, which gives

$$P = N_2N_1^{-1} = N_2 = X\Lambda X^{-1} \tag{7}$$

$$Q = Y\Lambda Y^{-1} \tag{8}$$

$$P = XY^{-1}QYX^{-1} \tag{9}$$

$$A = YX^{-1} \tag{10}$$

Therefore the error boxes can be calculated and we can get the T parameters of the DUT.

With reference to [19], the same microstrip open-end circuit was studied and the results confirm the remarks made from the SOC technique, as shown in Fig. 8.

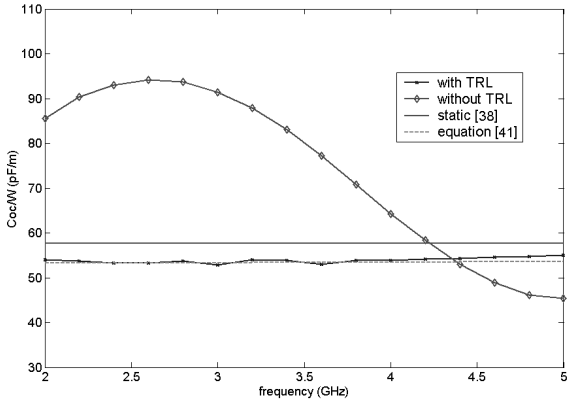

Fig. 8. TRL-extracted open-end fringing capacitance together with those obtained from the non-TRL parameter extraction scheme and two closed-form design equations (w = h = 0.635mm, ε_r = 9.9, L = 10.4 mm).

The standards used in the numerical TRL calibration are easy to realize. No strict requirement is imposed to know the exact reflection coefficient for the reflect standard, whose value can be determined during the calibration process. The numerical TRL technique does have some limitations. To achieve a best accuracy, the thru standard should be selected less than 1/4 wavelength while the line standard should be less than 1/2 wavelength at the highest frequency of interested range. Moreover, the electrical length difference between the two standards is required to be discernible, i.e., greater than 20°, at the lowest frequency. For a larger frequency range, multiple line standards must be applied. The standards and the simulated T-parameters are all based on the concept of TEM mode or quasi-TEM mode in our planar line simulation cases. The higher-order modes should be eliminated.

D. TR Calibration

The TRL calibration standards are simple and easily realizable in the numerical modeling. However, the calibration is valid over a limited 8:1 frequency range for one line standard. Multiple standards and calibrations should be applied for wide frequency calculations. The most critical problem is related to characteristic impedance of the Line standard in TRL calibration that should be known exactly [31]. Such limitations make the TRL calibration difficult and complex in the parameter extraction of planar discontinuities over a wide frequency band. A simple and straightforward approach called Thru-Resistor (TR) calibration technique was proposed in [32].

The TR calibration uses two standards: through and resistor. Like the SOC approach, the error boxes A and B are assumed to be reciprocal and symmetrical. Such properties are not general in the real measurement but general in the EM simulation. If A and B are not symmetrical, we can do two separate calibration procedures. The reciprocal property is valid for most of the microwave structure in simulation. TR calibration uses two standards, through and resistor. The resistor standard has a value of 2R. The connections of these two standards are shown in Fig. 9.

From the through connection, we can obtain 2-port admittance parameters, $[Y_T]$. As the error boxes are symmetrical, they should be terminated by a short or open if we make use of odd or even voltage sources at ports P1 and P2. We can thus obtain two input impedances at port P1 with Z_O and Z_S corresponding to open and short connections, respectively. Similarly, from the resistor connection we have 2-port admittance parameters, $[Y_R]$, and we can obtain input impedance Z_R. From Z_R, Z_O, and Z_S, we can write such impedance parameter equations of the error boxes as,

$$Z_{11} = Z_O \tag{11}$$

$$Z_{22} = R * \frac{Z_O - Z_R}{Z_R - Z_S} \tag{12}$$

$$Z_{12}^2 = (Z_O - Z_S) * Z_{22} \tag{13}$$

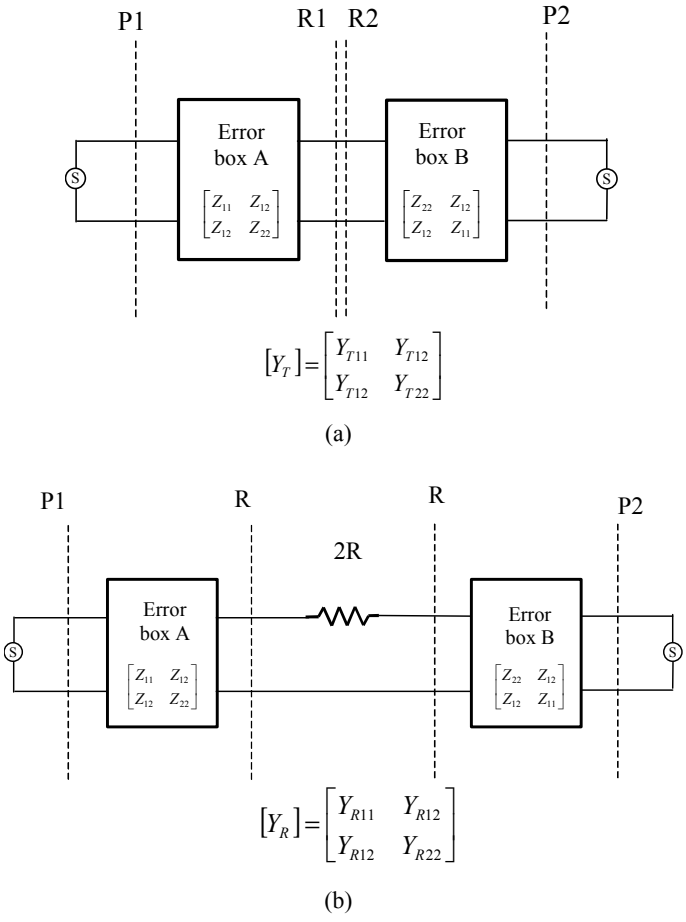

Fig. 9. Block diagram of the TR calibration procedure: (a) Through connection; (b) Resistor connection.

The example of a microstrip open-end was studied in [32] and the result confirms those generated from the TRL and SOC techniques.

In formulating this standard in a commercial MOM software, parasitic capacitance of the gap as well as effects of the via from the microstrip line to the resistor that can be considered as a serial inductance can bring up a little change in value of the resistor standards. The parasitic parameters of the resistor standard may bring error to the TR calibration, but it is much smaller than that in a real-world measurement.

III. APPLICATIONS

A. 3D characteristic impedance of transmission line.

Different two-dimensional (2D) definition of characteristic impedance of a transmission line can result in different value in an inhomogeneous media. Rautio [15][40] suggested a TEM equivalent impedance-3D definition in the modeling of a uniform line with finite length which is unique for any given transmission line geometry and is appropriate for use in circuit theory application. The definition uses ABCD-parameters of an ideal TEM transmission line

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j\dfrac{\sin(\beta l)}{Z_0} & \cos(\beta l) \end{bmatrix} \quad (14)$$

If the ABCD-parameters of a section of transmission line is known, Equation (14) can be used to evaluate Z_0 as well as the propagation constant.

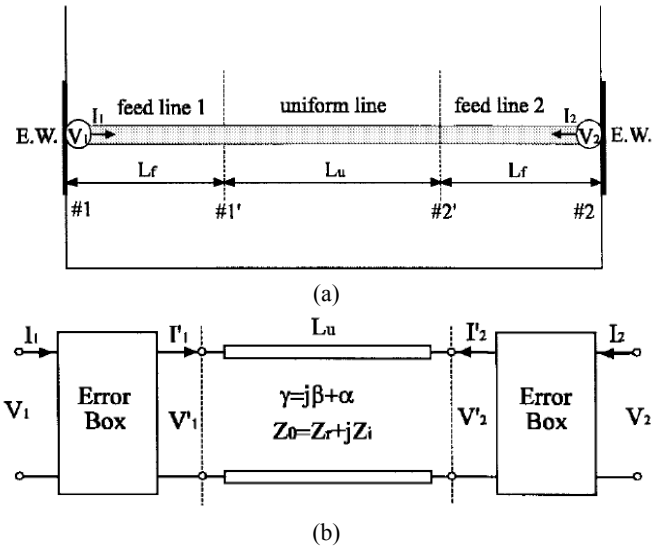

Fig. 10. 3-D model for the derivation of characteristic impedance of the uniform microstrip line with finite length L based on the self-calibrated IVS-MoM technique. (a) Physical model. (b) Equivalent network.

The SOC calibration was successfully used to generate the 3D parameters of a microstrip line [23] and the transmission line parameters of periodic coplanar waveguides (CPW) with inductive loads [22]. In [23], the uniform microstrip line was considered as the DUT as shown in Fig. 10. The results compared with the results obtained from the double-delay calibration are shown in Fig. 11.

In the TRL calibration, the calibration reference impedance, which is equal to the characteristic impedance of the line standards, should be known first. If there is error in characteristic impedance of the line standard, the use of equation (5) will cause error in the extracted parameters of the DUT. In [33], an additional resistor standard was implemented to determinate the 3D characteristic impedance of the line standard. The connection of the resistor standard is shown in Fig. 12.

The impedance of the resistor standard Z_t is chosen to be around the characteristic impedance of the line standard that can be calculated from a 2D method and the reference impedance of the TRL calibration procedure is chosen to be equal to Z_t. The 3D characteristic impedance of the line standard can be determined by solving the following nonlinear equation:

$$f(Z_x) = S_{11M} - S_{11MX}(Z_X) = 0 \quad (15)$$

where $S_{11MX}(Z_X)$ is the calculated input reflect coefficient of the network connected with a resistor Z_t after we obtain the error terms of the network from the TRL calibration, which depends on the reference impedance Z_X; S_{11M} is the value got from the simulation of the structure connected with the resistor standard using a MoM package.

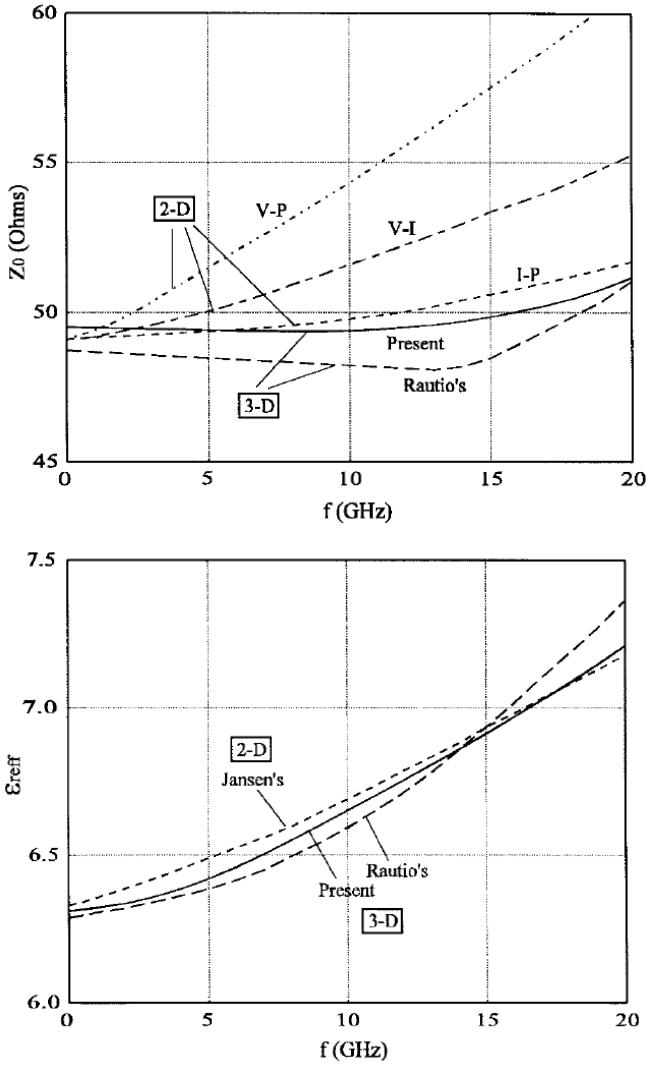

Fig. 11. Systematic comparison among simulated results on the characteristic impedance (Zo) and effective dielectric constant (ε_{reff}); given by the 2-D classical definitions, the 3-D Rautio's technique, and SOC technique for a microstrip line (w = h = 0.635 mm, ε_r = 9.7)

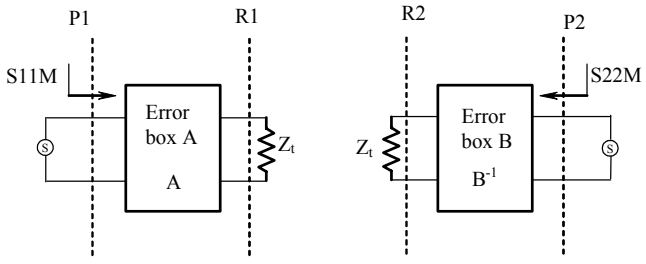

Fig. 12. The resistor standard connection used in the TRL calibration.

The characteristic impedance of a microstrip line was examined. In the example of calculation, the permittivity of substrate is 9.9, the substrate thickness and the line width are all equal to 0.635 mm. An electromagnetic simulator is used (Agilent's Momentum). The result is shown in Fig. 13.

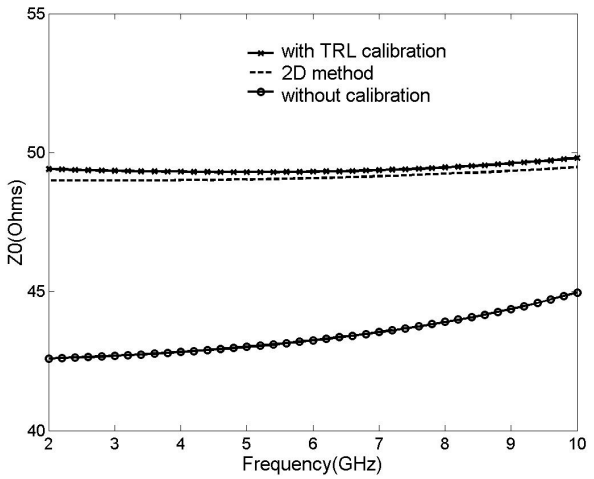

Fig. 13. Characteristic impedance of a microstrip line obtained from the improved numerical TRL method together with the data obtained without calibration and the data obtained from the 2D method ($\varepsilon_r = 9.9$, w = h = 0.635mm).

B. Planar discontinuities

With the calibration and de-embedding techniques described in section II, the errors brought by the port discontinuities and other factors can be removed and the parameters of simulated planar discontinuities can be accurately extracted. Based on the correctly extracted parameters, full-wave equivalent circuit model of the planar discontinuities can be built up.

Various microstrip discontinuities such as open-end [19] [31][32], gap [19] [32], step [18][33], interdigital capacitor [29], and others, were effectively extracted by using the SOC calibration and TR as well as TRL techniques, and the equivalent circuit models were then developed.

One example of the microstrip gap [19] is shown in Fig. 14. Interestingly, it is found that the simulated capacitances remain stationary over the frequency range of interest, while the simulated conductances move up exponentially with frequency. The results suggest that the capacitances defined in the equivalent network be really perceived as static parameters, which can be effectively calculated from a static field model. The increase in conductance indicates that the radiation loss becomes non-negligible as the frequency goes beyond 2.0 GHz for the specific structure. Naturally, the two sets of self-capacitance/conductance of the coupled structure are different from each other in view of its asymmetry. In addition, the self-capacitance/conductance, related to the larger line width W_2, is much more pronounced than its narrower line counterpart W_1.

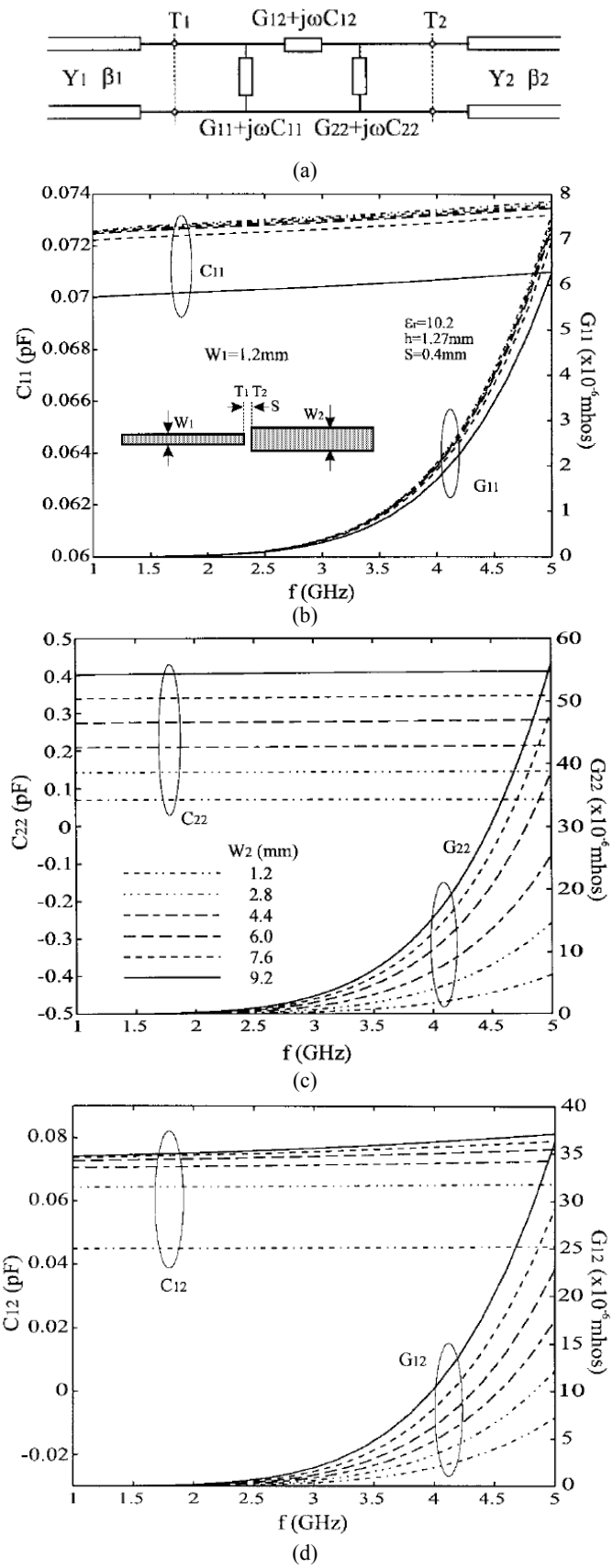

Fig. 14. Dispersion characteristics of the equivalent-circuit parameters for a gap discontinuity having unequal linewidths and different linewidth ratios. (a) generalized equivalent circuit model. (b) C11 and G11. (c) C22 and G22. (d) C12 and G12.

In [21], circuit models of some Coplanar Stripline Circuits (CPS) discontinuities were extracted by using the SOC technique, as shown in Fig. 15. Distinct features of the CPS discontinuities and circuits were presented with detailed results of the extracted circuit models. It was discussed and explained for the first time that the finite-ground line of unbalanced CPS structures may generate non-negligible and significant parasitic effects including an unexpected inductance effect or potential radiation loss or parasitic resonance phenomenon.

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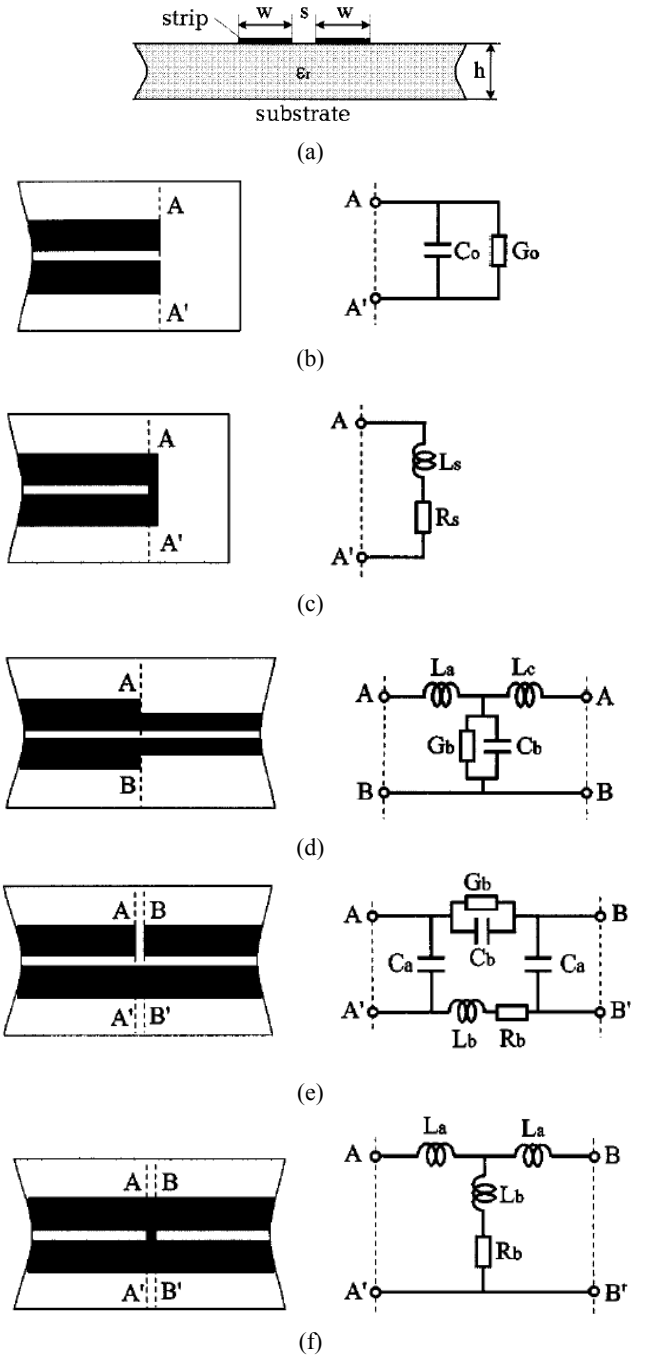

Fig. 15. Geometrical description, layout view, and equivalent circuit model of CPS circuits and discontinuities. (a) Cross section of a uniform line. (b) Open circuit. (c) Short circuit. (d) Step discontinuity. (e) Capacitively coupled circuit (gap). (f) Inductively coupled circuit.

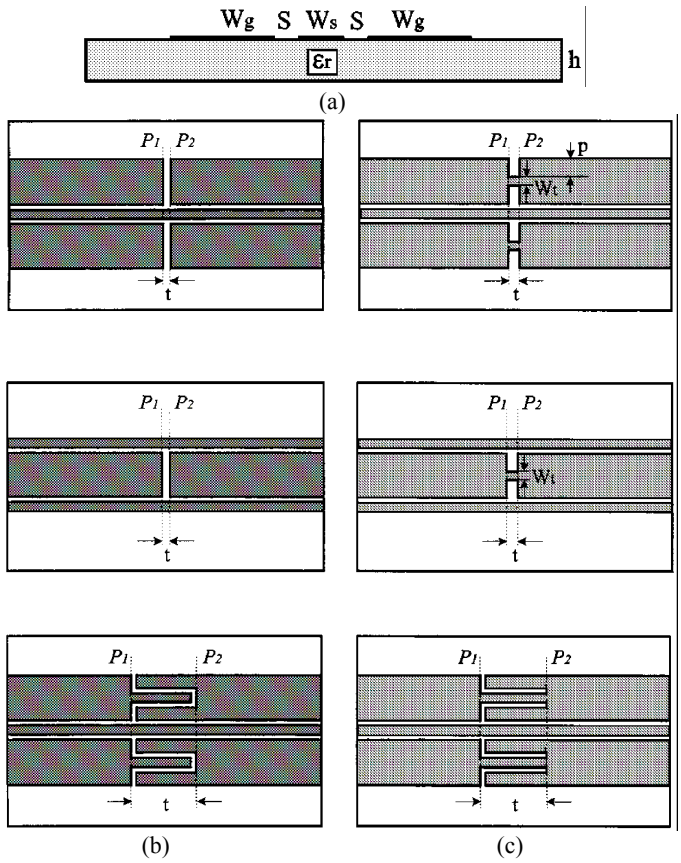

Fig. 16. Layout view of FGCPW reactive series-connected elements. (a) Cross section of FGCPW line. (b) Capacitive series element. (c) Inductive series element.

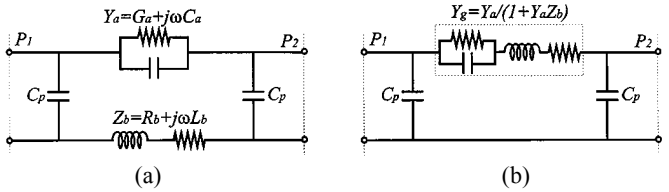

Fig. 17. Proposed computer-aided design (CAD)-oriented unified model of FGCPW capacitive series-connected elements, as shown in Fig. 16(b). (a) Initial circuit model. (b) Modified circuit model.

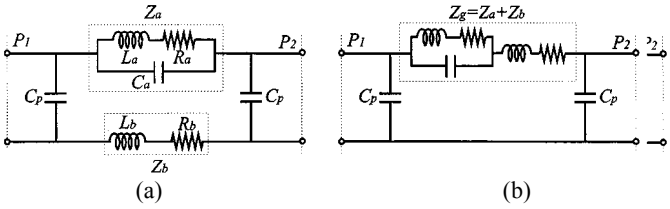

Fig. 18. Proposed CAD-oriented unified circuit model of an FGCPW inductive series-connected element, as shown in Fig. 16(c). (a) Initial circuit model. (b) Modified circuit model.

A variety of finite-ground coplanar waveguide (FGCPW) reactive series-connected capacitive and inductive elements were extensively studied and characterized as equivalent-circuit models that include complex parasitic effects caused by finite-ground widths, as shown in Fig. 16 [22]. The proposed model is generally described as an equivalent series

admittance or impedance together with a pair of shunt admittances for FGCPW series-connected structures, as shown in Fig. 17 and Fig. 18.

With the new scheme, the FGCPW elements of interest behave like lossless lumped elements at low-frequency range, consisting of a series capacitance or inductance, as well as two shunt capacitances. As frequency increases, however, the structures exhibit a frequency-related dispersion and also a lossy resonance behavior, which stand for some added inductive or capacitive coupling effect caused by the extent of finite-ground width. On the other hand, unbounded radiation effect, considered in this model, appears too strong to be ignored around resonance.

C. *Circuit design based on the full-wave model*

By using the calibration and de-embedding techniques, accurate full-wave equivalent circuit models of the planar discontinuities can be extracted as demonstrated in the previous section. That allows one to design a planar structure with conventional circuit-based fast synthesis and optimization.

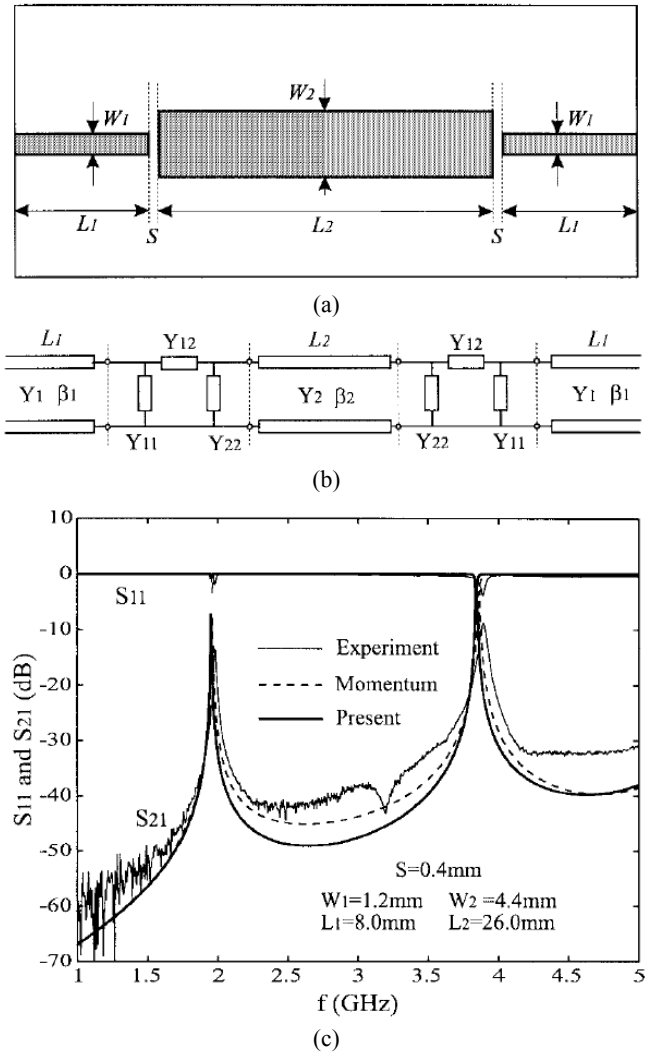

Fig. 19. A line resonator with unequal width of line/resonator (the input/output lines are identical in width). (a) Structure layout. (b) Equivalent-circuit model with cascaded elements. (c) The measured and simulated performance.

A microstrip-line resonator [19], as shown in Fig. 19(a), is poised to provide an accurate and useful assessment of the circuit model (in section B) in connection with the design/synthesis of a circuit having a number of cascaded discontinuities. To begin with, this line resonator structure is first segmented into several parts, and the simulated results presented in Fig. 14 for the gap discontinuities can be directly used in this example. Fig. 19(b) depicts an equivalent circuit model of the complete line resonator, which consists of two dynamic admittance π-networks for the gaps and a uniform equivalent transmission line effectively simulating the resonator. The complete transmission characteristics defined at the input/output ports of such a resonator circuit can be easily deduced from a simple circuit analysis. The relevant circuit samples are fabricated and measured. Fig. 19(c) pieces together the three groups of scattering parameters for the resonator having W_2=4.4mm. It can be seen that the proposed equivalent model gives very satisfactory results compared to the experimental results and simulated results of Momentum. Some very small difference between the simulations and measurements can be attributed to potential errors of fabrication tolerance and also experiment setup.

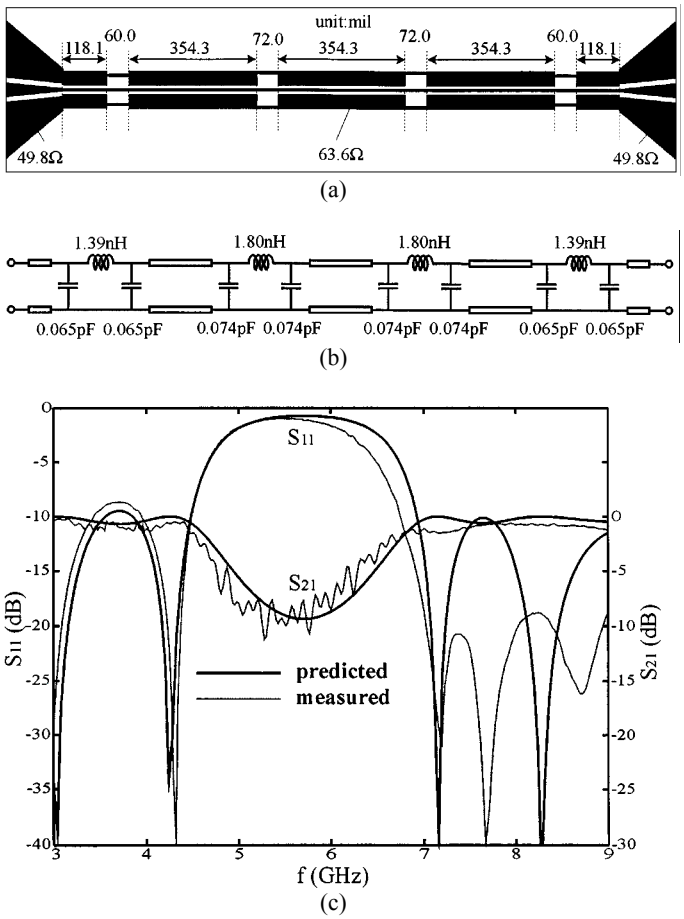

Fig. 20. An innovative uniplanar bandstop filter based on the wide-ground FGCPW inductive series-connected elements. (a) Detailed physical layout. (b) lumped-element circuit representation of the three-stage uniplanar bandstop filter (c) Predicted and measured performance.

With the SOC-extracted circuit model of a series FGCPW discontinuity shown in Fig. 16, an innovative filter design example is showcased with theoretical and experimental results for the uniplanar FGCPW structures [22]. Fig. 20 shows the layout and its complete equivalent-circuit model of a novel uniplanar multistage bandstop filter, in which each FGCPW line section represents an approximate half-wavelength uniform line resonator at the central frequency (5.8 GHz). Each FGCPW series element is characterized in terms of a lumped series inductance and a pair of shunt capacitance. On the basis of the circuit topology, as described in Fig. 20(b), the frequency response of such a filter can be modeled toward its specified electrical performance by applying a circuit network-based optimization procedure [39]. Fig. 20(c) shows its predicted electrical performance together with the measured results, which exhibit the Chebyshev-type bandstop frequency response. It is found that 3-dB frequency bandwidth with respect to the return loss is wider than 30%, while the insertion loss outside the stopband range appears to be smoothly varied around the ideal value of 0 dB.

D. Multi-port planar discontinuities

In the above discussions, a number of one-port or two-port examples have been provided. Multiport circuits can be modeled with the proposed SOC and TR calibration techniques without modifications. This is because each port can be handled independently. In [30], a multi-port SOC algorithm was elegantly formulated and implemented and a digital interconnect structure as shown in Fig. 21 was studied. The result is shown in Fig. 22. The coupled microstrip line 3-D characteristic impedance obtained by the multi-port TR calibration is also shown in Fig. 23.

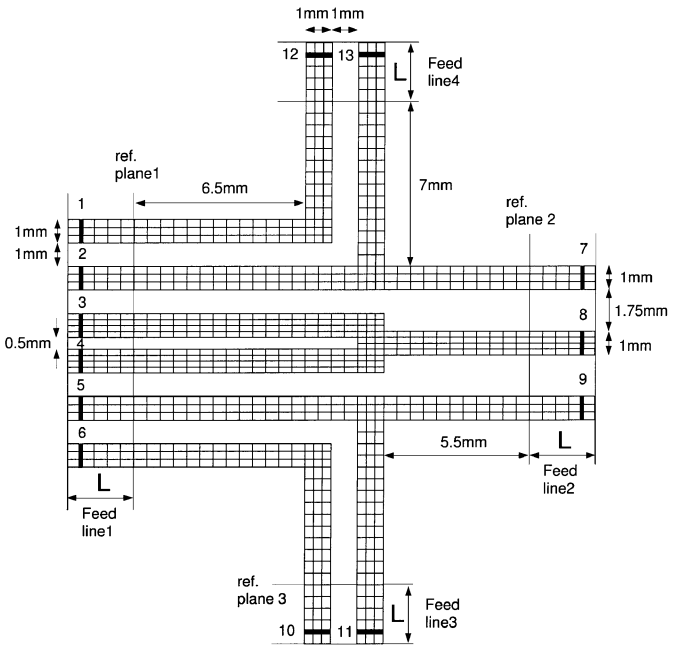

Fig. 21. Geometry and MoM discretization of a 13-port circuit.

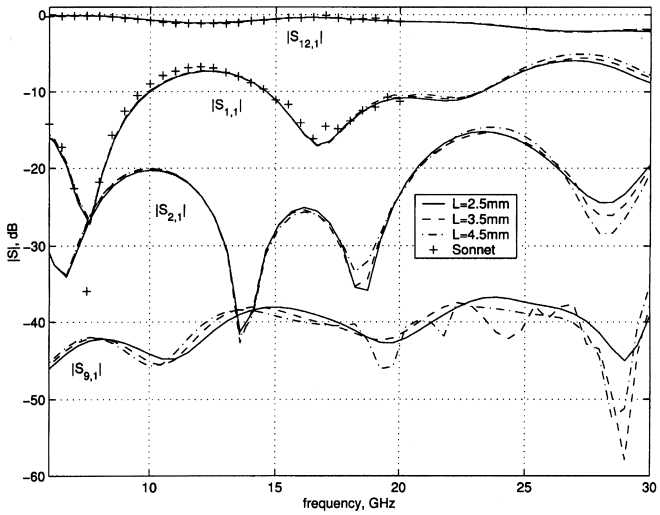

Fig. 22. De-embedded S-parameters for the 13-port circuit for different lengths L of the error boxes. The circuit is printed on a 0.7 mm thick grounded dielectric substrate of relative permittivity $\varepsilon_r = 3$.

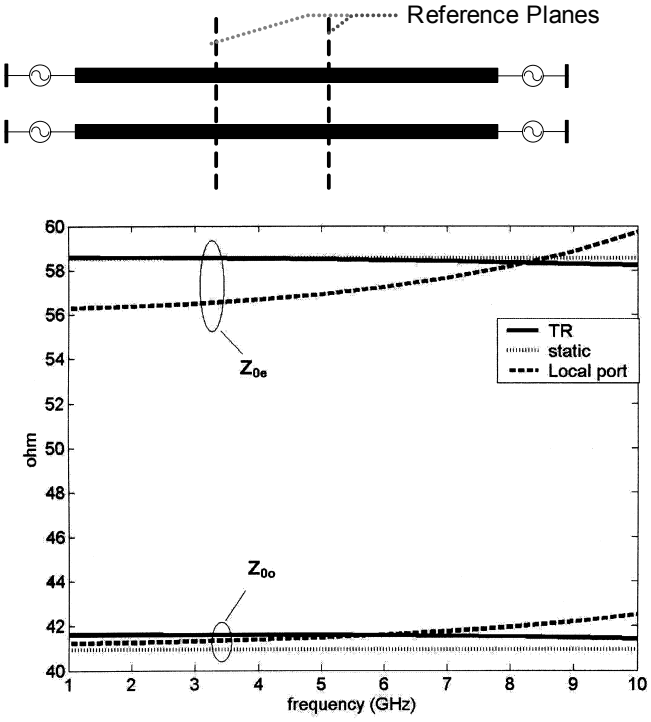

Fig. 23. 3-D characteristic impedance of a microstrip line obtained from multi-port TR calibration together with the data obtained without calibration (Local port) and the data obtained from the static method ($\varepsilon_r = 2.2$, w = 30 mil, h = 10 mil and s = 5 mil).

IV. CONCLUSIONS

In this paper, we have overviewed the state-of-the-art development in numerical calibration and de-embedding techniques that have been proposed and used in the full-wave electromagnetic simulation and modeling. These techniques are mainly proposed to solve the problem of "artificial" port discontinuities brought by the lumped current/voltage exciting source in the planar circuit simulations. A number of

standards similar to those used in real measurements as open, short, line, through, reflect and resistor are formulated in the different numerical calibration procedures. On the basis of such numerical calibrations and de-embedding techniques, one can accurately generate the full-wave equivalent circuit model of various planar microwave discontinuities and circuit elements, which can also give insight into the physical behavior of the structures. It has been demonstrated that those accurate models are critical in the design of innovative integrated circuits on the basis of well-established network design strategy for analysis and optimization. The proposed numerical calibrations and de-embedding techniques have been powerful and effective in bridging the gap between the field simulation and circuit design. Such concepts are not just limited to the modeling of electromagnetic problems; they can be well extended to other computational engineering discipline such as mechanical engineering.

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