A Novel Broadband Power Amplifier Using ATI

U. L. Rohde, A. K. Poddar, B. Bhat, M. Gurunathan

Abstract – **Designing a linear and wideband power amplifier had been a challenge in communication system design. Due to the restrictions on battery life, efficiency is an important design specification. High efficiency can also help to mitigate thermal issues. In this paper, we have explored the existing design practices and proposed some novel design methods to develop linear, efficient, high power amplifiers over a wide band.**

Keywords – **Wide band Power amplifier, TWA, ATI matching networks.**

I. INTRODUCTION

Power amplifiers are typically the most power-hungry building blocks of RF Transmitters and transceivers. Modern communications systems require highly linear power amplifiers, and to reduce the overall system cost, it is necessary to have a single broadband power amplifier, which can amplify multiple carriers. This puts an upper limit on the harmonic and distortion components. With improved efficiency the battery life increases and also reduces the cooling requirements for the same output power. For military and defence applications the power amplifiers are required to operate at elevated temperatures with very high reliability. Solid-state broadband power amplifiers with large output power bring down the cost and size of the overall system.

With the compound semiconductor processing technology getting mature and reliable [1], the power densities are reaching 10W/mm (of gate periphery) and higher. It is now possible to implement highly linear, broadband solid-state high power amplifiers, which can operate at high temperatures with high reliability.

II. EXISTING DESIGN TECHNIQUES

A. Limitations on wide band power amplifier designs.

1. Limitations of the class of operation

Class –A: The output characteristic of the power transistor along with the load line and bias point is shown in Figure 1. Equations (1) & (2) expresses the relation between optimum load ($R_{L,opt}$) and maximum output power ($P_{out,max}$) with device break down voltage (V_{br}), knee voltage (V_k) and drain saturation current (I_{DSS}) respectively. This configuration offers best linearity but poor efficiency.

Dr. Ulrich L. Rohde is the chairman of Synergy Microwave Corp and is a faculty member with University of Cottbus, BTU Cottbus 03046, Germany.
Dr. Ajay K.Poddar. is the chief scientist with Synergy Microwave Corp., NJ, USA and is a guest lecturer with TU, Munich, Germany, E-mail:akpoddar@synergymwave.com
Mr. B. Bhat, and Mr. M. Gurunathan are senior design engineers with Synergy Microwave Corp.

$$\boldsymbol{R_{L,opt}} = \frac{(V_{br}-V_k)}{I_{DSS}} \tag{1}$$

$$\boldsymbol{P_{out,max}} = \frac{(V_{br}-V_k)I_{DSS}}{8} = \frac{(V_{br}-V_k)^2}{8R_{L,opt}} \approx \frac{V_{br}{}^2}{8R_{L,opt}} \tag{2}$$

Tuned Class-AB/B: In class-AB (class B) operation the device is biased close to pinch-off (at pinch-off) point. The device amplifies for half cycle and remains cut-off for other half cycle. In tuned class-AB (class-B) sinusoidal output swings are obtained at the output by employing a resonator at the fundamental frequency thus impose a bandwidth restriction.

Class-E: Class-E and other switched mode amplifier architectures offer good efficiency. But they are highly nonlinear and cannot be used to achieve broad band amplifiers.

Doherty : Doherty architecture provides high efficiency and high linearity over a narrow band. The design is complex and cannot be achieved over a wide band. Also it requires hybrid power combiners, which is complex to implement in MMIC.

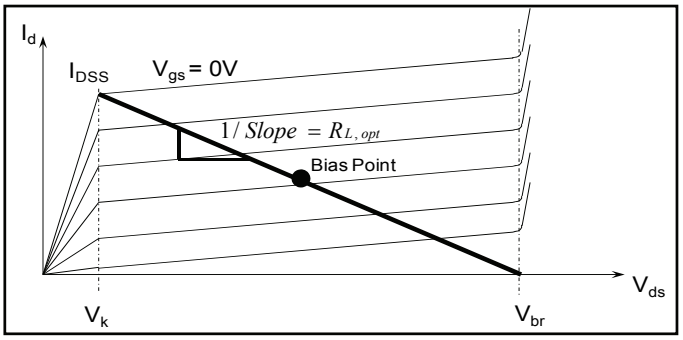

Figure 1. Showing the output characteristics and load line of a typical power transistor.

2. Limitation on load impedance

To increase the output power V_{br} has to be increased which means the device periphery has to be larger. Larger devices have smaller $R_{L,opt}$ (about 5Ω), designing a matching network to match $R_{L,opt}$ to 50Ω over a broad bandwidth is sometimes not feasible. Even if such a matching network is feasible it will be of a very large size.

3. Power frequency Limitations

The power frequency limit (pf^2) originates from the inherent limitation of the breakdown voltage that can be achieved by high frequency transistor technology. This limits the output power that can be obtained by the device over a broad bandwidth.

If E_{max} is the breakdown electric field in the semiconductor, then it can be shown that

$$f_T V_{br} \leq \frac{E_{max} v_{sat}}{\pi} \tag{3}$$

Equation (3) shows the trade off between the f_T(higher frequency of operation) and V_{br}(higher breakdown voltage). This trade off does not mean that high frequency devices have lower power. High output power can be obtained over narrow bandwidths at high frequency by matching the output to $R_{L,opt}$. But for a broadband amplifier from equations (2) & (3),

$$f_T{}^2 P_{out,max} \leq \frac{(E_{max} v_{sat})^2}{8\pi^2 R_{L,opt}} \quad (4)$$

4. Bandwidth limitations

Broadband high power amplifiers should use larger periphery low-f_T transistors (from equation (4)). Larger periphery transistor implies higher gate capacitance (C_{gs})

$$C_{gs} = \frac{G_m}{2\pi f_T} \quad (5)$$

G_m the large signal transconductance of the device is given by

$$G_m = \frac{I_{Dss}}{V_P} \quad (6)$$

The higher C_{gs} causes difficulties in designing broadband input matching networks thus limiting the bandwidth of the high power amplifiers. This can be overcome by reducing the $G_{m,extrinsic}$ by capacitive or resistive degeneration (which reduces the gain of the amplifier), but still the gain bandwidth product is limited by f_T.

5. Limitations on gain

Higher gain is needed for higher efficiency. The following are the definitions of the two efficiencies

Drain Efficiency:- is the DC to RF conversion efficiency is defined as the ratio of the RF output power (Pout) to the DC power drawn from the drain supply

$$DE = \frac{P_{out}}{P_{DC,D}} 100\% \quad (7)$$

This is the amount of DC power that gets converted in RF power.

Power Added Efficiency (PAE):- is the ratio of the difference of the RF output power and the RF input power (Pout- Pin) to the DC power drawn from all the supplies (PDC).

$$\text{PAE} = \frac{(P_{out} - P_{in})}{P_{DC}} 100\% = \frac{P_{out}}{P_{DC}} \left(1 - \frac{1}{G}\right) 100\% \quad (8)$$

Where G is the power gain of the amplifier. Since the PAE accounts the RF drive for the output power amplifier stage, it is a representative of the overall system efficiency compared to the output power amplifier. A low PAE due to low gain of the amplifier means that the efficiency of the driver amplifier also significantly affects the overall system efficiency.

B. Wide band Amplifier Design

The amplifier designs discussed previously employ frequency selective matching networks that couple power to the device effectively over a narrow bandwidth. Distributed or Travelling wave amplifiers (TWA) by absorbing input capacitance (C_{gs}) into a synthetic input (gate) transmission line. This synthetic transmission line introduces delays among various transistors of TWA. A similar output (drain) synthetic transmission line provides compensating delays at the output circuit, so that ac currents of all the transistors add in phase at the load. The high bandwidths are observed primarily because of absorption of C_{gs} into input synthetic line (since $C_{gs} > C_{ds}$).

In the synthetic output transmission line, the AC drain current of each transistor contributes equally to forward and reverse travelling waves. At low frequencies, the lengths of the delay line are negligible and each device is matched to its optimum load. Due to significant delays at higher frequencies, the reverse waves do not add up in phase. So the power lost in the reverse transmission is smaller. However the load-line seen by the device is far from optimum due to the same reason resulting in lesser output power and efficiency. This issue would be addressed with the proposed improvised TWA architectures.

III. ATI BASED MATCHING NETWORKS

We propose an innovative technique of using active tuneable inductor (ATI) for matching networks in power amplifier applications.

A. Active Tuneable Inductor (ATI)

ATI is an inductor realized using active elements like transistor and it can offer a variable inductance with an applied DC tuning voltage. This would allow tuning of the circuit after fabrication [2]. ATI has very low loss and even exhibit negative resistance in certain cases.

1. Conventional ATI

The typical active inductor is based on gyrator, which can be realized by connecting inverting amplifier to non-inverting one in parallel and back-to-back. The electronic gyrator (Figure 2) converts capacitor C into the inductance L. The phase compensating network improves the dynamic range of ATI.

$$L(v) \approx \frac{C}{g_{m1} \times g_{m2}} \quad \text{(Ideal Case)} \quad (9)$$

Drawbacks of this configuration are as follows.

- Real part of the input impedance is positive everywhere (i.e. $\text{Re}\{Z_{in}\} > 0$) and hence lossy
- Care must be taken to avoid encircling and crossing point. i.e. 4.3GHz (#3) in figure 3.
- Only shunt inductors possible i.e. one terminal of the inductor needs to be grounded.

2. Improved ATI

A novel ATI with SiGe HBT was developed with negative real value of impedance. Hence these ATI's are loss less. ATI in SiGe technology (figure 4) has been successfully demonstrated. Investigations will be carried out for ATI implementation in GaN and other MMIC technologies.

MMIC inductors are very lossy and they occupy a large real estate in the chip. This makes the matching networks lossy as well as larger in size. With the proposed technique of using

ATI in matching networks, the losses can be reduced (figures 5& 6). Since the transistor occupies lesser area than inductors, the size of the chip gets reduced. Figure 7 below shows the broadband matching network implemented using ATI.

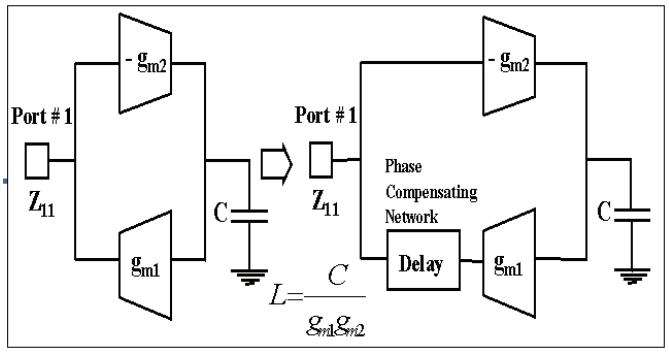

Figure 2. Showing typical equivalent representation of gyrator based active inductor

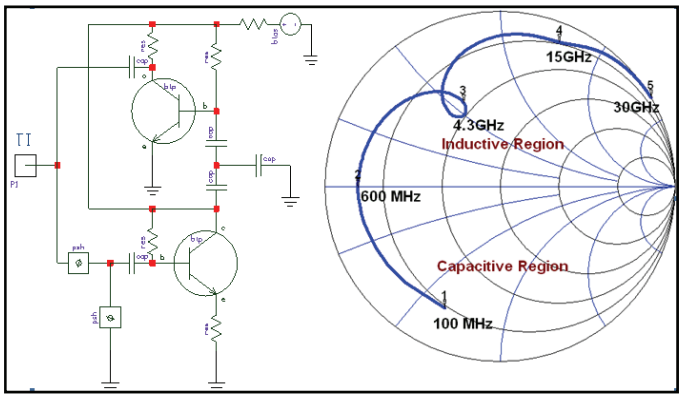

Figure 3. A typical schematic of active inductor and its corresponding impedance plot

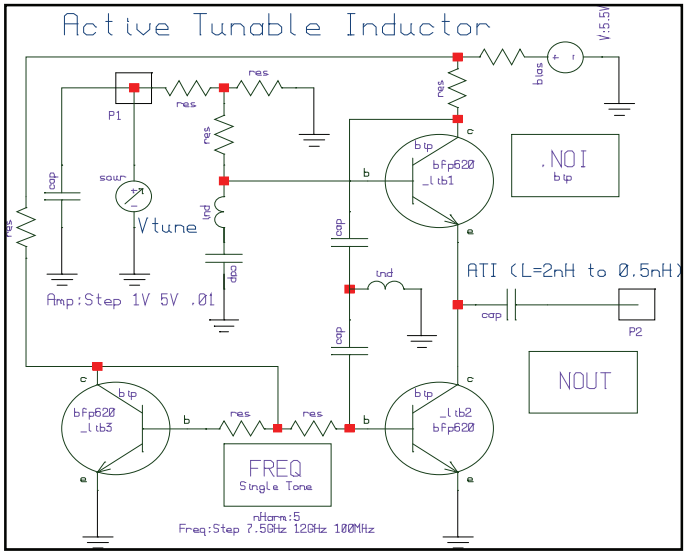

Figure 4. Showing a typical schematic of the ATI using bipolar (Infineon BFP 620).

ATI's reported so far have been plagued by the disadvantage of a very poor dynamic range, especially if the ATI had to be used for matching networks in power amplifiers. Currently, work is being carried out to improve the dynamic range of ATI.

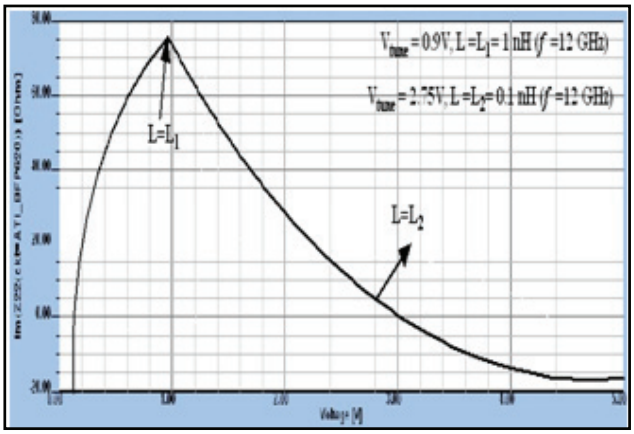

Figure 5. Typical plot of reactive impedance (imaginary part of Z_{22}) at port 2

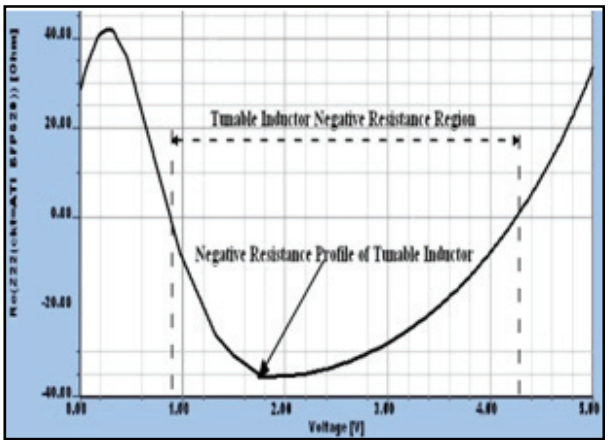

Figure 6. A typical plot of resistive impedance (real part of Z_{22}) at ATI port.

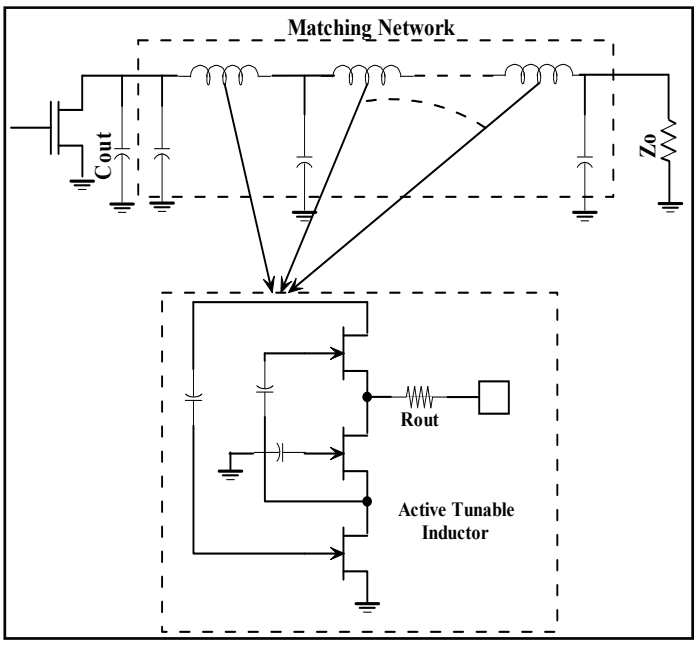

Figure 7. Showing schematic of broadband matching network using ATI.

IV. TWA CONFIGURATIONS

A. Conventional TWA configurations

Distributed amplifier circuits can operate over a very large bandwidth with high gain bandwidth product. TWA stands distinct among other alternatives owing to its wide-bandwidth. Since the individual stages in a TWA operate in class-A or class-AB, these amplifiers are inherently linear. We have built a travelling wave amplifier giving a flat gain of 14dB from 20MHz to 2.5 GHz. The fabricated amplifier and the corresponding measured results are shown in figure 8a, 8band 8c.

Travelling wave amplifiers are popularly used for designing high power, wide bandwidth power amplifiers. But they are highly inefficient. The reasons for their inefficiency are discussed in detail in the following sections.

The gain of a TWA is calculated by adding the contribution from each transistor stage. For a TWA with N transistors, the gain is given by

$$\left|\frac{V_{out}}{V_{in}}\right| = \left(\frac{-gmZo}{2}\right)\sum_{n=1}^{N} e^{\left[-\left(\frac{n-1}{2}\right)(\alpha_g+j\beta_g)-\left(\frac{N-n+1}{2}\right)(\alpha_d+j\beta_d)\right]} \quad (10)$$

Where αg, αd are the attenuation per line section and βg, βd are the phase constants of gate and drain lines respectively.

1. Limitations of the conventional TWA

Limitations on the bandwidth of TWA are given by K.Krishnamurthy et al [3] and are summarised as follows.

Delay mismatch between gate and drain lines.

By assuming loss less lines (α_g=0, α_d=0), the gain expressions simplifies to

$$\begin{aligned}\left|\frac{V_{out}}{V_{in}}\right| &= \left(\frac{gmZo}{2}\right)\left|\sum_{n=1}^{N} e^{[-j(n-1)2\pi f\Delta\tau]}\right| \\ &= \left(\frac{gmZo}{2}\right)\left|\frac{1-e^{[-j2\pi fN\Delta\tau]}}{1-e^{[-j2\pi f\Delta\tau]}}\right| \\ &= \left(\frac{gmZo}{2}\right)\left|\frac{e^{j\pi fN\Delta\tau}-e^{-j\pi fN\Delta\tau}}{e^{j\pi f\Delta\tau}-e^{-j\pi f\Delta\tau}}\right| \\ &= \left(\frac{gmZo}{2}\right)\left[\frac{\sin(\pi fN\Delta\tau)}{\sin(\pi f\Delta\tau)}\right] \\ &= \left(\frac{NgmZo}{2}\right)\left[1-\frac{(N2\pi f\Delta\tau)^2}{24}\right] \end{aligned} \quad (11)$$

where higher order terms of fΔτ are ignored in the last approximation. The gain decreases with higher frequency because the transistor outputs no longer add in phase. Hence it is necessary to design the gate and drain lines to have equal delays in order to eliminate the bandwidth limits arising due to delay mismatch.

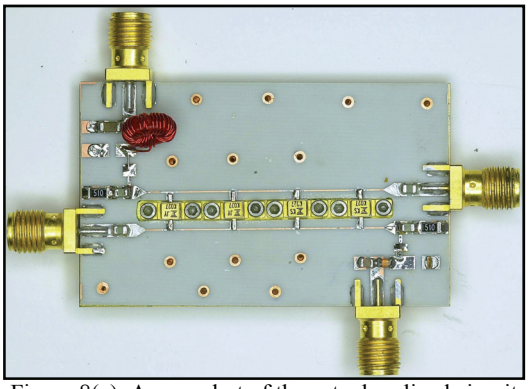

Figure 8(a). A snap shot of the actual realized circuit

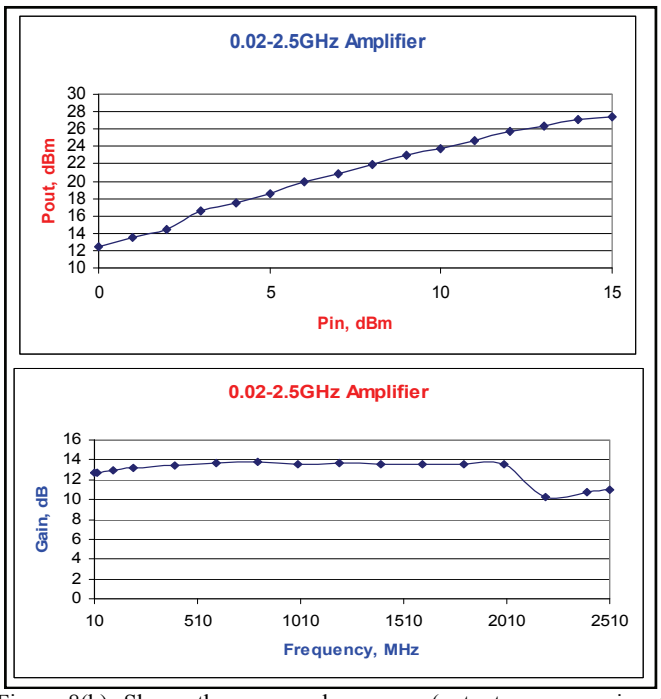

Figure 8(b). Shows the measured response (output power vs. input power, gain vs. frequency) of the TWA

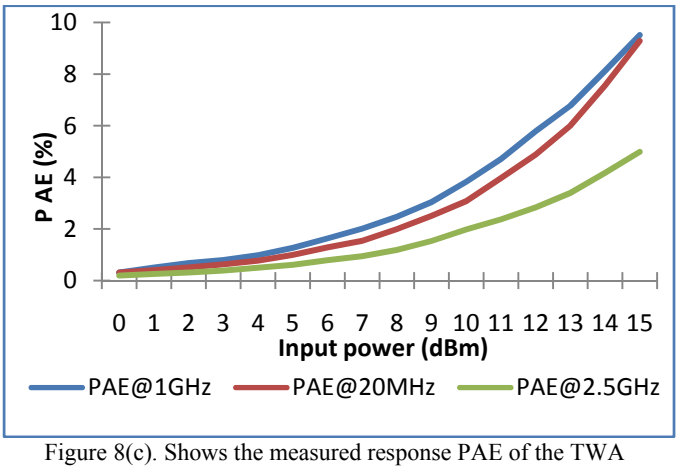

Figure 8(c). Shows the measured response PAE of the TWA

Figure 8. (a) Shows a snap shot of the actual realized circuit, (b) Showing the measured response of the TWA and (c) Showing the measured response PAE of the TWA

Gate line attenuation

The input voltage of N^{th} transistor is attenuated by $e^{-(N-1/2)\,\alpha g}$. To keep the loss in the gate drive of the N^{th} transistor within 1dB, we require,

$$\mathbf{N\alpha_g \equiv N.\frac{4\pi^2 f_{high}^2 c_{gs}^2 r_i Z_o}{2} \leq 1/8,}$$
$$\mathbf{f_{high} \approx \frac{1}{M}\frac{1}{4\pi C_{gs}\sqrt{R_i Z_o}}} \quad (12)$$

where M is the degeneration ratio.

Thus the gate line attenuation is independent of the number of cells for a given net periphery and could be varied only from degeneration.

Drain line attenuation

The output of the first transistor is attenuated by $e^{-(N-1/2)\,\alpha d}$ before it reaches the output. To keep the attenuation within 1 dB in the drain line, we should have

$$\mathbf{N\alpha_d \equiv \frac{Z_o}{2r_{ds}} \leq \frac{1}{8}} \quad (13)$$
$$\mathbf{\frac{Z_o}{R_{ds}} \leq \frac{1}{4}\ (capacitive\ degeneration)} \quad (14)$$
$$\mathbf{M\frac{Z_o}{R_{ds}} \leq \frac{1}{4}\ (Resistive\ degeneration)} \quad (15)$$

Hence for the given net periphery, the drain line attenuation is independent of the number of cells. Resistive degeneration is advantageous compared to capacitive division because it reduces the drain line losses.

Reasons for lower efficiency in conventional TWA

1)Improper distribution of power among cells especially the cells at the end of TWA structure receives very low power.

2)Backward travelling wave in drain line:

To eliminate this, drain line tapering is done. In general a TWA with N cells and load Z_O, requires output line sections of impedance NZ_O [3]. The problems with large impedance line are (1) it is difficult to realize in MMIC and (2) the current carrying capability of the line decreases (3) it is highly lossy, thus rendering the implementation of drain line tapering impossible for 50Ω load.

3)All cells are biased evenly and not according the maximum voltage swing.

4)Improper absorption of C_{DS}, which results in lower efficiency, lower output power and lower bandwidth

B.Improved TWA Configurations

1. Use of Cascode Delay matched cells in TWA

The cascode delay matched TWA is a transadmittance-transimpedance pair consisting of a tapered drain line transadmittance (common-source) stage driving a low input impedance common-gate transimpedance stage. Successive cascading of transadmittance-transimpedance stages results in strong impedance mismatch between stages. This principle is frequently used in high gain broadband systems. Impedance mismatch makes the intermediate nodes low impedance in nature thereby minimizing the RC charging times and improving the bandwidth. Besides improvement in efficiency there are other advantages of CDM TWA. In cascode stage most of the output voltage swing appears across CG device. This allows the use of low breakdown and high f_T device for CS stage and high breakdown device for CG Stage.

A dual gate device is electrically equivalent to a common source (CS) / Common gate (CG) cascode pair. As explained previously, the CS device determines the stage bandwidth and CG device determines the breakdown voltage in a cascode. Thus a dual gate device designed with CS device having short L_g (gate length) for high f_T and CG device with larger L_g for higher V_{br} can provide simultaneous high f_T and V_{br} required for broadband applications. This does not violate Johnson's limit but just splits the bandwidth and breakdown requirements between CS and CG device [6]. This technique could lead to a significant increase in the efficiency of the amplifier. Figure 9 shows the proposed amplifier with dual gate cells.

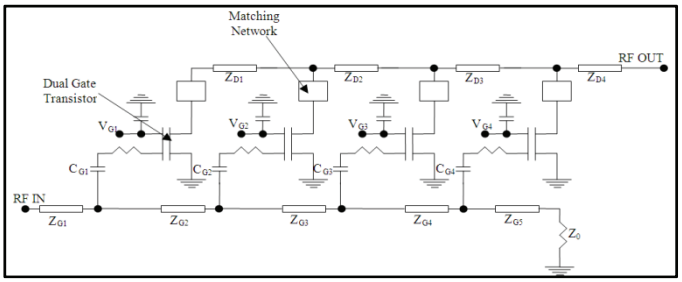

Figure 9. Schematic of proposed TWA with dual gate cells.

2. Individual biasing & class-AB biasing of stages

The individual stages have to be ac coupled and biased according to the voltage swing. The efficiency can be further improved by biasing the stages in class-AB mode without much compromise with linearity. Also, the individual stages can be biased such that the distortion components have out of the phase gains and hence get cancelled at the output [5].

3. TWA with CG output stage

The CG stage acts as a low impedance load broadband impedance transformer with an impedance transformation ratio of $(V_p/(V_{br}-V_k))$ and a bandwidth of f_T. This reduces the backward travelling wave in the drain line thus improving the output power and efficiency. The width (W_2) of the CG output is chosen according to $W_2 = 4 * W_1$.

Broadband C_{DS} matching networks absorbs the transistor parasitic and presents optimal load impedance to the transistor. The losses in the matching networks can be reduced with the use of ATI. The presence of CG output device makes the drain line tapering more feasible. This increases the output power and the efficiency of the amplifier. The formula given below gives the impedances of the drain lines

$$Z_{D1} = Z_S, Z_{D2} = \frac{Z_S}{2}, Z_{D3} = \frac{Z_S}{3}, Z_{D4} = \frac{Z_S}{4} \quad (17)$$
$$Z_S = \frac{NV_pZ_O}{V_{br}-V_k}$$

The circuit shown in figure 10 was simulated and the results are shown in figure 11. The simulation results show that the

proposed amplifier would improve the efficiency to up to 42% which is very impressive.

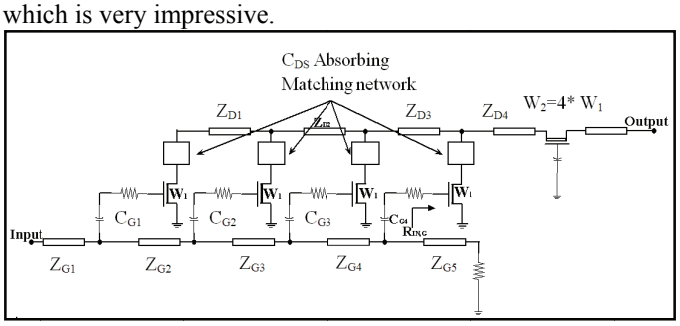

Figure 10. Schematic of the proposed TWA.

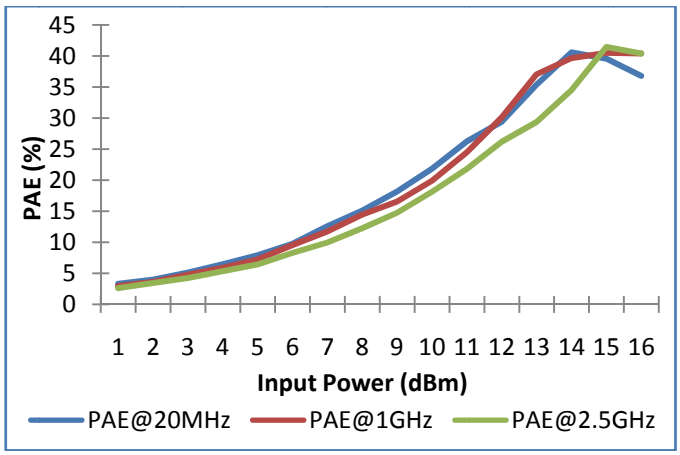

Figure 11. Shows the simulated PAE of the proposed TWA

V. Improved Class-A Amplifier

Figure 12 shows the schematic for the proposed class-A amplifier with dynamic bias control. The proposed class-A amplifier (with dynamic bias control and broadband matching network using ATI) overall has better efficiency than the conventional class-A amplifier.

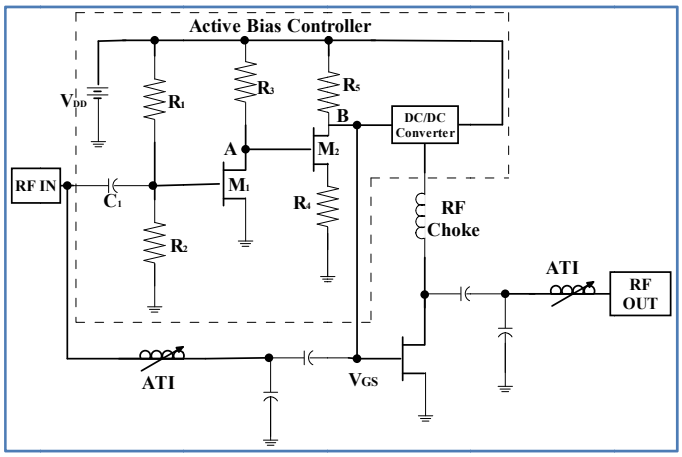

Figure 12. Schematic of proposed class-A amplifier with dynamic bias control and matching network using ATI.

A. Dynamic control of biasing

If a power amplifier can be operated at higher back-off, the efficiency can be improved by reducing the bias voltage and current of the transistor(s). In dynamic bias control, the quiescent current and bias voltage of the power device is changed according to the input power [7][8]. At low power levels, the quiescent current is made low to reduce the DC power consumption and thereby to increase the efficiency. The overall efficiency can be significantly achieved using dynamic bias control in class-A amplifier. The equations below suggest that V_{GS} can be determined based on output power (P_{out}).

$$\begin{aligned} R_{L,opt} &= \frac{Voltage\ Swing}{Current\ Swing} \\ V_{knee} &= (V_{GS} - V_{TH}) \\ P_{out} &= \frac{(V_{br}-V_{knee})^2}{2R_{L,opt}} = \frac{(Voltage\ Swing)^2}{2R_{L,opt}} \\ I_D &= \sqrt{\frac{2P_{out}}{R_{L,opt}}} \\ G_m &= \frac{I_D}{V_{GS}-V_{TH}} \\ V_{GS} &= \frac{1}{G_m}\sqrt{\frac{2P_{out}}{R_{L,opt}}} + V_{TH} \end{aligned} \tag{18}$$

The use of DC/DC converter (figure 12) is proposed to vary the V_{DS}. Figure 13 shows the variation of the way in which dynamic bias control works by varying the V_{ds} and I_d when the device is operated at higher back-off levels thus reducing the power consumption in the device. C_1 & M_1 are the coupling capacitor and detector respectively for the input signal. The sizes of C_1 and M_1 should be as small as possible to minimize the effects on the input matching circuit. R_1 and R_2 are bias resistors of M_1, and the bias voltage is designed close to its threshold voltage.

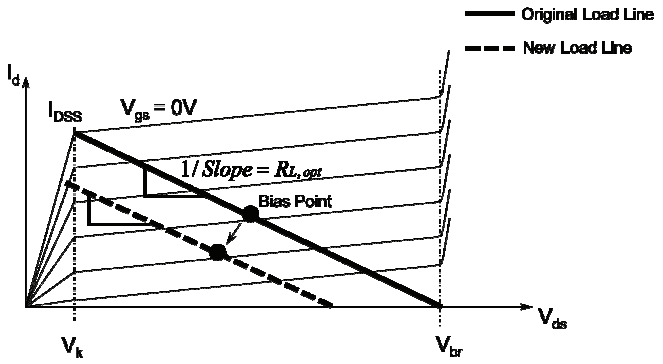

Figure 13. Showing the concept of dynamic bias control with the original and new bias points

When input RF power increases, it leads to an increased harmonic in the drain current of M_1, and it causes the voltage to decrease at node A and at the meantime the voltage at node B raises the bias voltage of the power transistor. Figure 14 demonstrates the input power versus voltages at node A and node B. At high input power levels the distortion at node B is high, but the high C_{GS} of the power transistor forms an

effective low pass filter which shorts out all the distortion components [8].

The figure 15 below shows the simulated results for the circuit shown in figure 12. The circuit was designed to operate at 1GHz with a small signal gain of 12dB and DC power dissipation 1W. It can be seen that the overall efficiency of the amplifier is significantly improved and the maximum efficiency is close to 31% which is impressive for class-A amplifier.

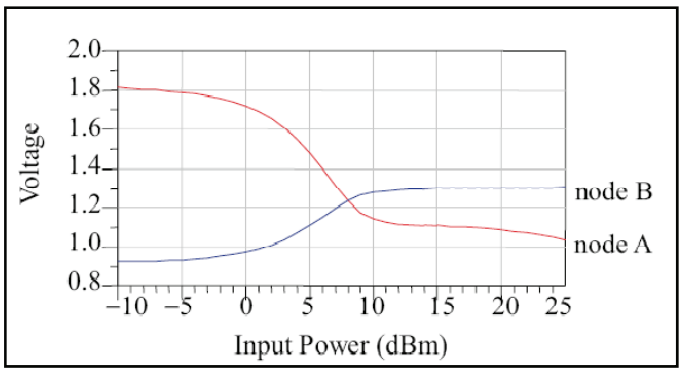

Figure 14. The input power versus node A and node B.

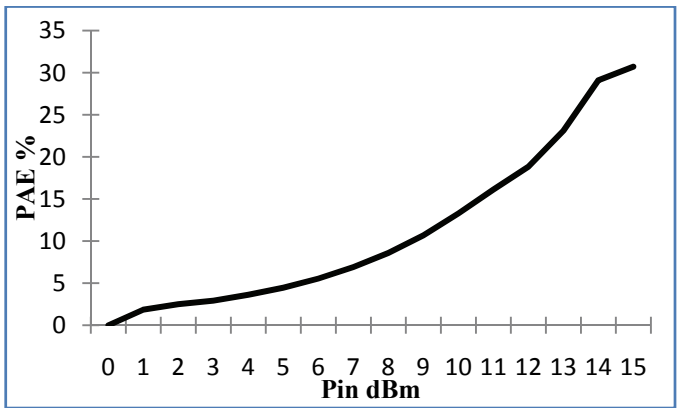

Figure 15. Figure showing the simulated PAE of the circuit shown in the figure 12 at 1GHz.

VI. CONCLUSION

The basic amplifier configuration and the limitations involved in designing wideband power amplifiers have been reviewed. TWA amplifier configuration was found to be best suited for designing wide band power amplifiers although they suffer from poor efficiency.

A novel idea of using ATI for designing matching networks was proposed. The conventional ATI topologies and its drawbacks have been reviewed. Newer techniques have been proposed to improve the losses associated with ATI. A novel ATI was successfully developed in SiGe HBT technology and attempts are being made to improve the dynamic range of ATI.

The ultimate goal is to perform a comparison of a conventional TWA with an improved TWA employing ATI based matched networks. As a first step, a TWA was designed and fabricated. It was found to give a flat gain of 14dB from 20MHz to 2.5GHz. Various improvements of the basic TWA employing ATI based matching networks, have been proposed and some preliminary design and simulations were performed. A class A amplifier employing ATI based matching networks and dynamic bias control has been proposed to improve the efficiency of the amplifier.

REFERENCES

[1] Robert J. Trew, Daniel S. Green and Jeffrey B. Shealy "AlGaN/GaN HFET Reliability", *IEEE Microwave magazine*, vol. 10, no. 4 June 2009.

[2] U. L. Rohde and A. K. Poddar, "Tunable Active Inductor Offers Integrable and Cost-Effective Alternatives of Varactor Tuned VCOs", *2009 European Frequency & Time Forum & IEEE Int'l Frequency Control Symposium (EFTF-IFCS 2009)*, Besançon, France, April 20-24 2009.

[3] K. Krishnamurthy, R. Vetury, S. Keller, U.K. Mishra, M. J. W. Rodwell, S. I. Long, " Broad-band GaAs MESFET and GaN HEMT Power amplifiers", *IEEE Journal of Solid State Circuits*, Sep.2000.

[4] K. Krishnamurthy, S. I. Long, M. J. W. Rodwell, (Edited by: M. Matloubian, E. Ponti), "Cascode-Delay-Matched Distributed Amplifiers for Efficient Broad-band Microwave Power amplification", *IEEE 1999 Microwave and Millimeter wave Monolithic Circuits Symposium Digest*, 1999, pp. 819-822.

[5] Hitoshi Sumi at. el., " Ku-Band, 120-W Power Amplifier Using Gallium Nitride FETs", *IEEE International Microwave Symposium 2009*, pp. 1389-1392.

[6] C.-H.Chen, K.Krishnamurthy, S.Keller, G. Parish, , M.Rodwell, U.K.Mishra, Y.-F. Wu. "AlGaN/GaN dual-gate modulation doped field effect transistors", *Electronics letters*, vol. 35, no.11, 1999, pp.933-935

[7] Kyounghoon Yang, Jack R. East and George I. Haddad "Automatic control of Efficiency and linearity of power amplifiers for low power wireless communications", *IEEE Silicon Monolithic Integrated Circuits in RF Systems 1998*, pp. 113-118, 17-18 Sep 1998, Ann Arbor, MI, USA.

[8] Fun Ye, Jen-Shiun Chiang, Chun-Wen Chen and Yu-Chen Sung, "Dynamic Bias Circuits for Efficiency Improvement of RF Power Amplifier", *Tamkang Journal of Science and Engineering*, vol. 7, no 3, pp. 183-188 2004.