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CMOS Instrumentation Amplifier: Comparative Analysis and Design for Enhanced Performance in Diverse Applications

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Abstract – **In this study, we explore diverse CMOS instrumentation amplifier designs tailored for industrial and biomedical applications, culminating in an enhanced version with superior characteristics, including high gain, exceptional common-mode rejection ratio (CMRR), and improved gain bandwidth. Instrumentation amplifiers (INAs) employed in sensing nodes need to be cost-effective without requiring trimming and should be energy-efficient, particularly in the context of Internet of Things applications. However, achieving this goal remains challenging. The design process involves the initial implementation of an operational amplifier (Op Amp) to realize the instrumentation amplifier (INA). The input stage employs two basic Op-amps, and the output stage is subjected to analysis through four different configurations. Various techniques, such as using two or three op-amps, employing a difference amplifier at the output stage, incorporating current feedback, and utilising capacitively coupled or capacitive neutralization methods, are investigated. Our selection criteria prioritize a high-precision instrumentation amplifier with considerations for CMRR, gain, minimized unwanted noise, and reduced power dissipation. The entire design and simulation process is executed on Cadence Virtuoso 180nm Technology. Notably, the modified INA exhibits a significantly improved gain of 125.57 dB and a high CMRR of 147.2556 dB compared to alternative designs, showcasing its enhanced performance.**

Keywords – **Operational Amplifier (Op-Amp), Folded Cascode, Instrumentation Amplifier (INA), Offset Voltage, Common Mode Rejection Ratio (CMRR).**

I. INTRODUCTION

In In the modern era of wireless communication, the role of advancement and exploration of CMOS technology is significant among several other techniques. It may be possible to embed a whole device on a single chip with a low-cost, miniaturised structure with low-voltage and minimum-noise circuitry [1-3]. A basic Op Amp can strengthen weak signals as well as noise elimination. Unlike operational amplifiers, INA is a type of differential amplifier that has a closed-loop gain block in which there is no need for matching input impedances as buffer amplifiers are present at the input of INA [4-5]. Amplification of weak signals with the elimination of unwanted noise suppression of CMRR can be performed by INA [6-9]. This is used in many applications such as micro-electromechanical systems, signal acquisition systems, transducers, Internet of Things (IoT) bio-potential instrumentation amplifiers and many more bio-medical systems [10-12].

Nowadays, there is a huge demand for portable and wearable gadgets so that continuous monitoring can be done on health or vital signals such as blood pressure, electrocardiography (ECG), electroencephalography (EEG), etc [13-15].

High-precision instrumentation should have the following properties such as high gain, greater CMRR, low offset voltage drift & offset voltage, high-value input impedance & well-matched, low noise, simple gain selection and low non-linearity [21-25]. Since these parameters rely on each other. For Internet of Things (IoT) applications, there is a preference for solutions that are economical, energy-efficient, have minimal noise, and exhibit rapid start-up settling. Therefore, it's a difficult task to develop a suitable highly precise instrumentation amplifier topology, which can obtain a reduced unwanted noise, high common mode rejection ratio (CMRR) high gain, with less power dissipation [26-30].

The formation of this paper is as follows: The insight of the basics of operational amplifier and operation is demonstrated in Section 2. A summarized analysis of instrumentation amplifier (INA) topology is described in Section 3. A comparative study of different configurations is explored in Section 4, and this contains all of the crucial information including gain, CMRR, gain bandwidth, noise figure and power dissipation. Lastly, the conclusion of the survey is enunciated in Section 5.

II. OPERATIONAL AMPLIFIER (OP-AMP)

In this Section, the basic block design of INA is discussed i.e. operational amplifiers. In Fig.1, the block diagram of the basic Op-Amp & in Fig. 2, the transistor level diagram is described.

Three aims were explicitly carried out using the obtained methodological technique:

Step 1: Design the circuit shown in Figure 2 and determine the element values such as aspect ratio(W/L) and compensated capacitor (Cc).

Often these analogue circuits and systems include operational amplifiers.

Step 2: The circuit should be analysed and the circuit's characteristics, including common mode rejection ratio (CMRR), DC gain (A_v), & power supply rejection ratio (PSRR), and should be calculated.

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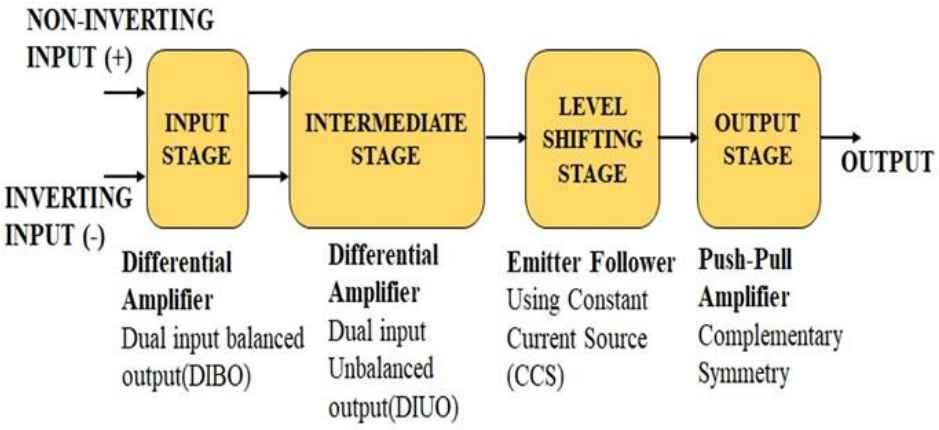


Fig. 1. CMOS realization of a two-stage operational amplifier

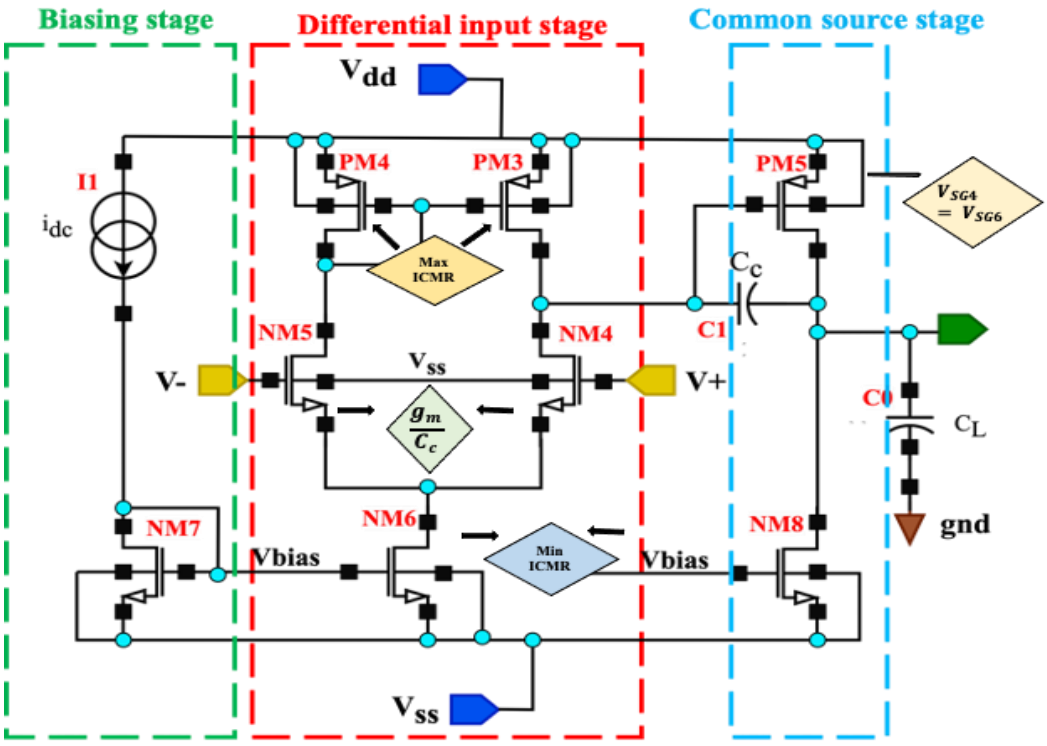


Fig. 2. CMOS realization of a two-stage operational amplifier [2]

Final Step: The design was observed to satisfy the main Characteristics of Op-amp [31-34]:

i) Open Loop DC Gain
ii) Slew rate
iii) CMRR
iv) -3dB bandwidth
v) Output swing
vi) Unity gain bandwidth

Also, mostly needed in high-functioning switched-capacitor filters & ADC are both high unity gain bandwidth as well as high DC gain [35-37]. To design a high gain and high-bandwidth op amp, the most popular method is a gain boost architecture in which gain can be easily improved rather than compromising Op-Amp's bandwidth [39]. Since single-stage fully amplifiers have fewer poles than multiple-stage Op Amps, they can reach higher unity gain frequencies [40-42].

III. INSTRUMENTATION AMPLIFIER

This section provides an overview of the basic INA which is employed in many industrial and biomedical applications. With the advancement of microelectronics & embedded systems, an increasing number of applications need very weak signal detection & measurement. This problem can be overcome by using INA so that any undesirable noise or common-mode signals can be eliminated which affect the basic signal & it furthermore provides appropriate amplification to the preferred signal [43-45].

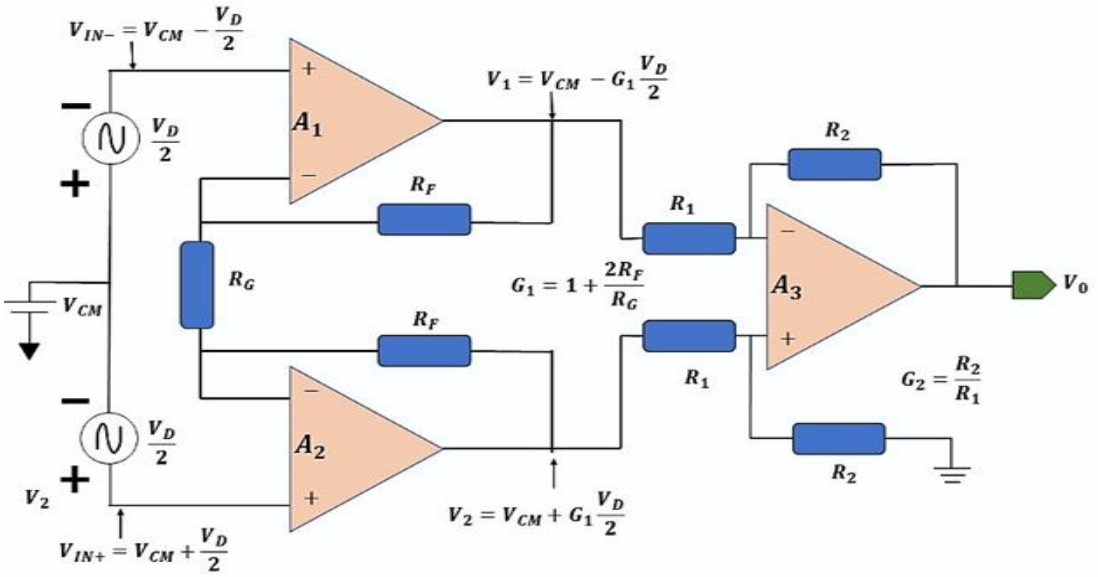


Fig. 3. Three op-amp instrumentation amplifier [10]

The standard 3 op-amp INA is presented in Fig. 3 [10]. the input stage of INA $\boldsymbol{A_1}$ and $\boldsymbol{A_2}$ has input polarities $\boldsymbol{V_{IN-}}$ and $\boldsymbol{V_{IN+}}$ followed by differential amplifier $\boldsymbol{A_3}$. These inputs of INA can be given as follows Eqs. (1):

$$V_{CM} = \frac{\boldsymbol{V_{IN-}+V_{IN+}}}{\boldsymbol{2}} \;\&\; V_D = V_{IN+} - V_{IN-}. \tag{1}$$

In terms of difference voltage & common-mode, the input voltage is calculated as Eqs. (2) :

$$V_{IN+} = V_{CM} + \frac{V_D}{2} \;\&,$$
$$V_{IN-} = V_{CM} - \frac{V_D}{2} \;. \tag{2}$$

To calculate Current I_D , difference voltage is applied across the gain resistor

$$I_D = (V_{IN-} + V_{IN+})/R_G = \frac{V_D}{R_G}, \tag{3}$$

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D.R_F \;,$$
$$\&\; V_2 = V_{CM} + \frac{V_D}{2} + I_D.R_F. \tag{4}$$

Substitute I_D value of Eqs. (4) from Eqs. (3)

$$V_1 = V_{CM} - \frac{V_D}{2} * G_1 \;,$$
$$\&\; V_2 = V_{CM} + \frac{V_D}{2} * G_1, \tag{5}$$

where Gain, $G_1 = 1 + (2 * \frac{R_F}{R_G})$.

The V_D is intensified by gain and the common-mode voltage has been passed through the input stage alongside unity gain.

After the second stage, the output of the difference amplifier is expressed by

$$V_0 = (V_2 - V_1) * G_2 \;, \tag{6}$$

$$\text{where } G_2 = \frac{R_2}{R_1}$$

The transfer function of INA can be calculated using Eqs. (5) and (6) and gives Eqs. (7)

$$\frac{V_0}{V_D} = G_1 * G_2 = G_{TOTAL}. \tag{7}$$

Due to mismatching of the resistor, INA suffers from a restricted value of CMRR. The output stage of a standard INA uses a unity-gain difference amplifier which could restrict the input common range consequential. To improve CMRR, a switched capacitor INA can be used but it has a poor input impedance.

IV. Different Topologies of Instrumentation Amplifier (INA)

To realize a better performance of INA in amplifying signals, different topologies were proposed by many researchers for intensifying signals to well-matched levels while refusing undesirable common-mode signals. Five topologies are going to be scrutinized within the subsequent section, comprising the first including the first local current feedback INA[16], active resistance INA [17], 3-stage INA which includes 2 simple op-amps with a folded cascode [18], modified 3 op-amps using differential amplifier which becomes the common approach in biomedical applications as well as low power sensor application [19], and therefore the recently reported CMOS INA which is based on traditional INA replaced 7 resistors with NMOS in triode region[20].

A. Local current feedback INA
B. Active CMOS instrumentation amplifier
C. OP-Amp with folded cascode
D. Modified INA using differential amplifier
E. Area efficient CMOS INA

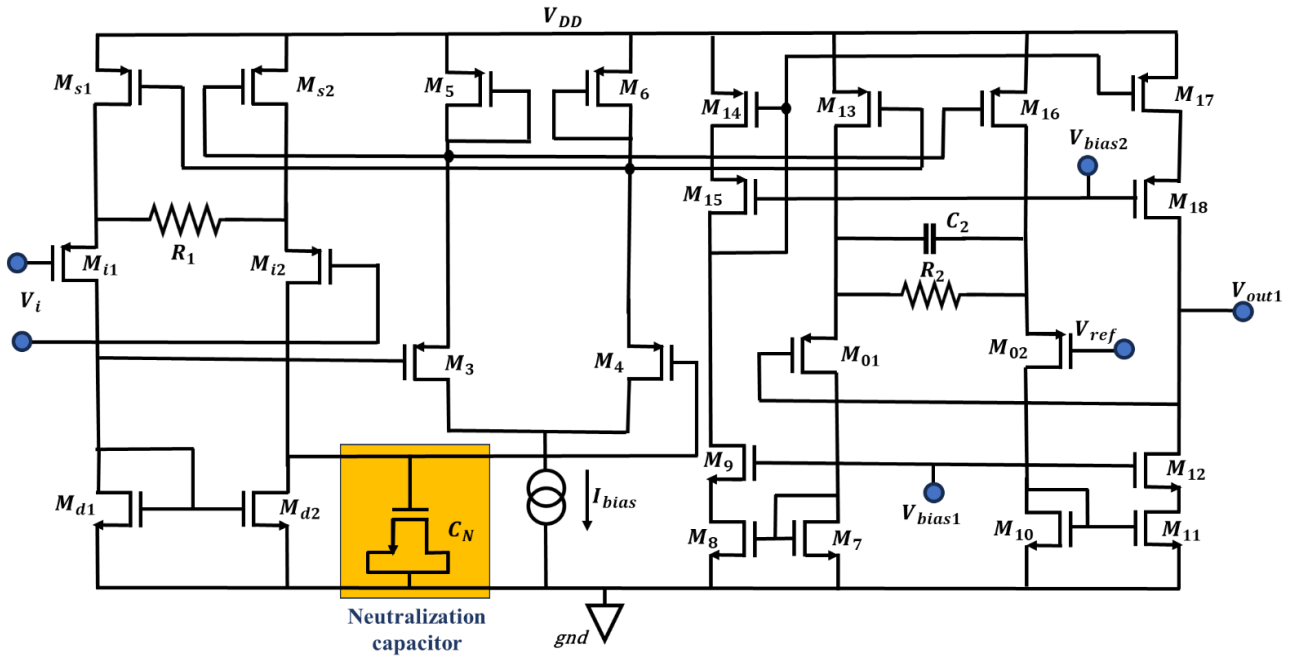


Fig. 4. Schematic diagram of INA using neutralization capacitor C_N to balance the drain capacitances of the input pair transistor [16]

A. Local Current feedback INA

In this topology [16], CMOS INA is implemented with 90 dB CMRR using a capacitive neutralization technique. From low to high frequencies, an overview of the common-mode gain frequency responses of the local feedback INA topology caused by discrepancies in the transconductance, drain-source capacitance, and the parasitic capacitance parameters in input level (up to about 10 MHz) has been discussed in this topology. Furthermore, the systemic discrepancy between the INA's drain capacitance and the current-mirror load is the primary cause of low CMRR at high frequencies. To relieve this impact, it has utilized capacitive balance and exhibited its adequacy from the manufactured CMOS INA chip tests, accomplishing a normal CMRR >90 dB up to the circuit's (2 MHz) bandwidth. This is the finest high-frequency CMRR output for a CMOS INA with minimal current utilization ever recorded. Fig. 4 depicts the schematic diagram of INA using the neutralization capacitor C_N to balance the drain capacitances of the input pair transistor [16].

B. Active CMOS Instrumentation Amplifier (INA)

In this topology [17], CMOS INA is implemented for the recording of weak-frequency biomedical signals with DC-suppressed high-gain INA. It is a three-op-amp configuration which provides high input impedance, initially, two op-amps are employed in the buffer layout and differential arrangement is utilised in the output stage. The NMOS transistors $\boldsymbol{M_1}$, $\boldsymbol{M_2}$, $\boldsymbol{M_3}$, $\boldsymbol{M_4}$, $\boldsymbol{M_5}$, $\boldsymbol{M_6}$, **and** $\boldsymbol{M_7}$ are operated in triode mode through the application of DC voltages $\boldsymbol{V_{BIAS1}}$, $\boldsymbol{V_{BIAS2}}$, $\boldsymbol{V_{BIAS3}}$, $\boldsymbol{V_{BIAS6}}$, and $\boldsymbol{V_{BIAS7}}$. These voltage values are calculated using Eq. 8. A Major drawback of INA is that an adequate performance depends on resistors of INA and fabrication requires a large chip area of all-inclusive INA with passive resistance. Passive resistance design of INA is not a precise method due to their consumption of large areas and high dependency on temperature imposes serious implications. Therefore, the passive resistance of INA is replaced by an NMOS transistor in triode mode to make it an active INA.

$$r_d = \frac{L}{K\prime W(V_{gs}-V_t)}. \tag{8}$$

The proposed active INA circuit is given in Fig. 5 [17].

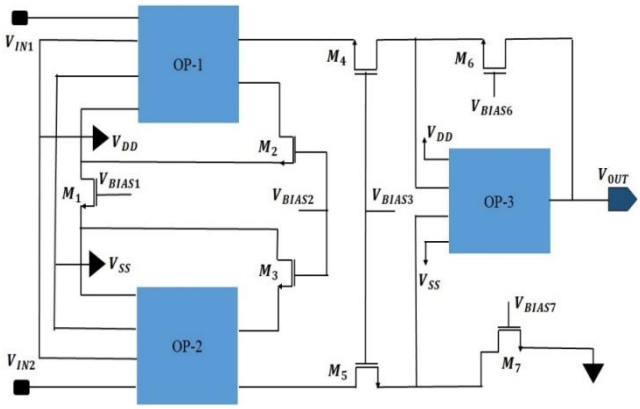


Fig. 5. Block diagram of active CMOS INA [17]

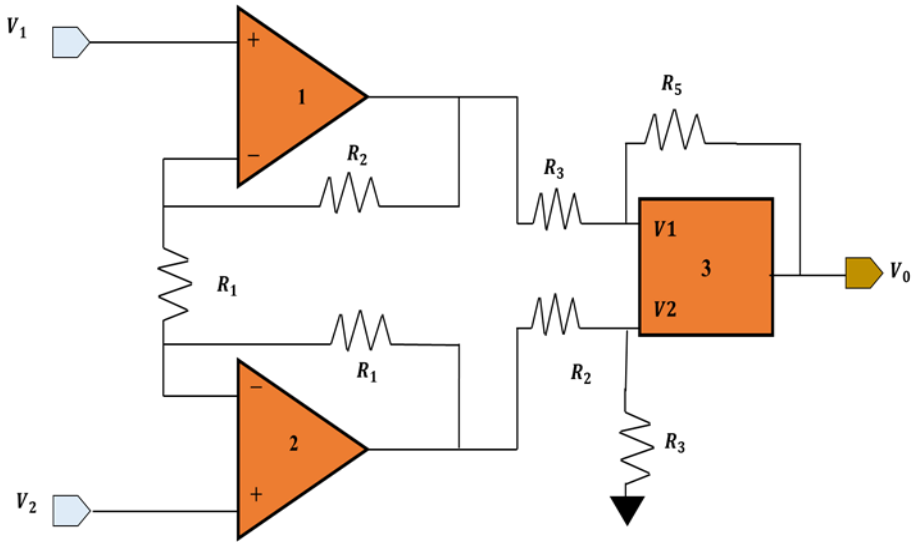


Fig. 6. Instrumentation amplifier circuit [18]

C. OP-Amp with Folded Cascode

In this topology [18], CMOS INA is Implemented with novel improved gain and minimum noise for applications of bio-medical such as ECG signal handling. A conventional 3 stage INA as shown in Fig. 6 is planned by utilising two basic Op-Amps at the two input stages and at the output stage, folded cascode Op-Amp is used. The layout of INA is drawn on both on & off-chip resistors. Utilising a folded cascode Op-Amp at the output stage has considerably enhanced the value of gain and the value of CMRR. The major benefit of utilising a folded cascode at the output stage of design is that without affecting the output swing, the gain can be expanded further. Optimum transistor sizing plays a very important norm in designing INA for bio-medical applications. While developing INA, the major worry is the disruptions brought on the common mode voltages. To achieve high input impedance, two input Op-Amps are utilised in a buffer configuration, and then a folded cascode two stage Op-Amp is employed in differential setup. Due to non-linear behaviour of folded cascode Op-Amp, which results into reduced DC gain, special consideration was taken at input to operate differential pair in saturation region instead of the triode mode. Each input op-amp in the system exhibits a gain of 45 dB and a CMRR of 72 dB. The folded cascode amplifier in the output stage achieves a CMRR of 92 dB and a gain of 82 dB. Consequently, the overall design attains a total gain and CMRR of 67 dB and 92 dB, respectively. With a modest power consumption of 263µW, this instrumentation amplifier proves to be particularly suitable for applications in biomedical signal processing. A configuration of on-chip resistors with and without illustrates that with on chip burned-through more region than without on chip as well as gain can be controlled externally with off-chip resistors.

D. Modified INA using a differential amplifier

In this proposed topology [19], INA is proposed for low-power portable monitoring systems whereas preserving high CMRR, high gain, minimal noise and considering additional constrictions as well. A 1.8 V power supply with a bias current of 20 µA is employed in this instrumentation amplifier analysis. At the input stage, INA contains 2 identical 2 stage Op-Amps operating in the saturation mode & at the output stage One differential amplifier in subthreshold mode is operating. The resistive network parameters for the IA are illustrated in Fig. 7, denoted by R_G, R_F, R_1, and R_2, with values of 1000 ohms, 100 milliohms, 10 kilohms, and 1 milliohm, correspondingly. To maintain transistors in saturation mode and Subthreshold mode, the aspect ratio plays a crucial role. For low power sensors applications, different transistor sizing is unveiled. The IA achieves a CMRR of 98 dB and an overall gain of 79.16 dB. This specific design of the instrumentation amplifier operates with a total power consumption of 409 µW and exhibits an input referred voltage noise, rendering it well-suited for low-power sensor applications and biomedical signal processing. The main problem is to reduce interferences while designing INA which are as a voltage that is a common-mode. In future scope, the amplifier's noise and offset can be decreased while sustaining the required design constraint.

I. Area Efficient CMOS INA

In this instrumentation amplifier design [20], an improvised version of CMOS INA is implemented with high gain and area efficiency for VLSI applications. As well as differential amplifiers and op-amps have also been designed in this work. This circuit is favourably considered for a design of the System on Chip architecture (SoC) which can be integrated with any sensor. Two Stage Op-Amp was designed, where the first stage is a differential amplifier & next stage is a common

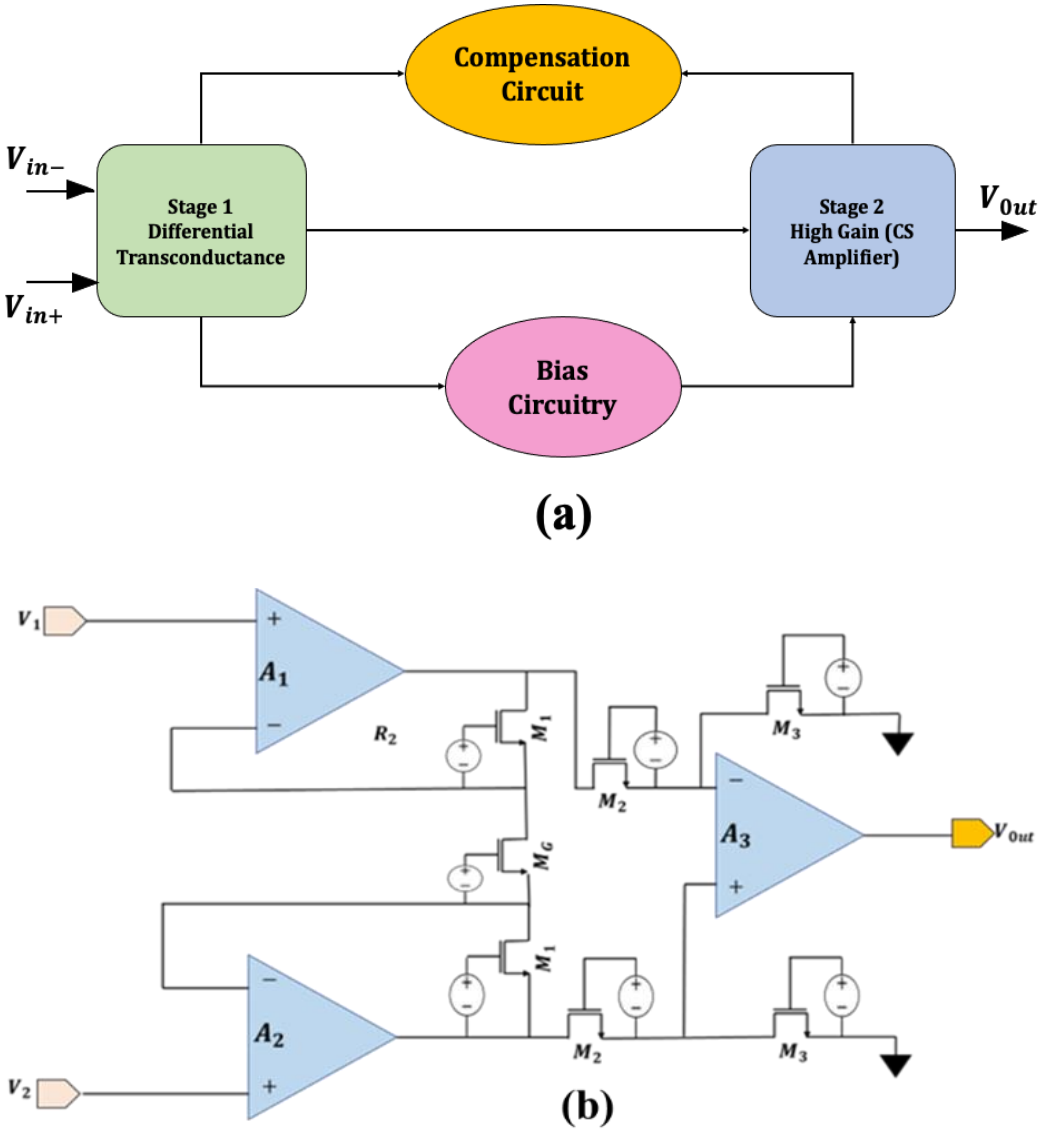


Fig. 8. (a) Block diagram of basic operational amplifier, (b)Schematic diagram of area efficient instrumentation amplifier [20]

source (CS) amplifier. A basic 2 stage Op-Amp consists of 4 blocks:

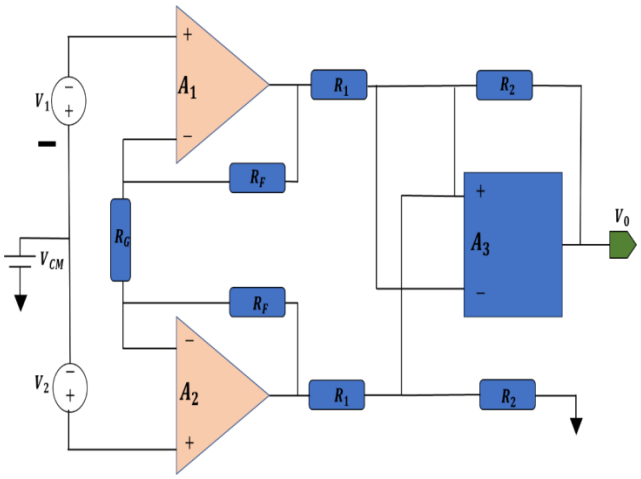


Fig. 7. Block diagram of modified instrumentation amplifier [19]

A differential transconductance configuration is present at the input level, after that a common source (CS) amplifier is utilised at the second stage, which provides a large output-swing for a given supply voltage while maintaining a high DC gain and biasing circuitry as depicted in Fig. 8(a)**.** In this work, INA is designed using three op-amps configuration. In a typical instrumentation amplifier, resistors occupy a significant portion of the chip's area. Fig. 8(b) illustrates a modification in the proposed circuit where NMOS components replace resistors in the triode operating region. This substitution leads to a reduction in occupied area. The circuit's power usage stands at 4.85 milliwatts. A closer examination demonstrates that the proposed CMOS instrumentation amplifier achieves a gain of 95.59 decibels, a CMRR of 108.4 decibels, and a measured gain bandwidth of 3.95 MHz. For reduction of area, seven resistors of op-amps are replaced by NMOS in triode mode. The simulation was carried out utilizing the Cadence Analogue Design Environment with UMC 90nm technology, and the proposed design functions on a 1.8 V power source. High gain, high

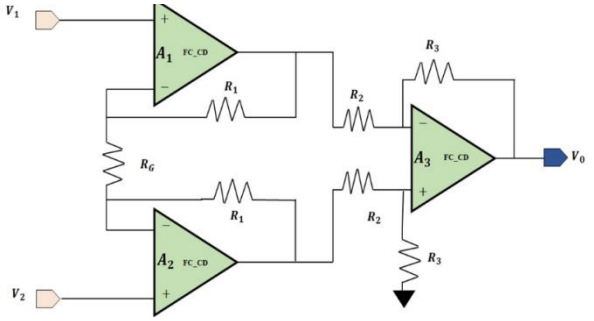
CMRR and low power consumption are noted in this research article.

V. Proposed Instrumentation Amplifier (INA) with Folded Cascode Topology

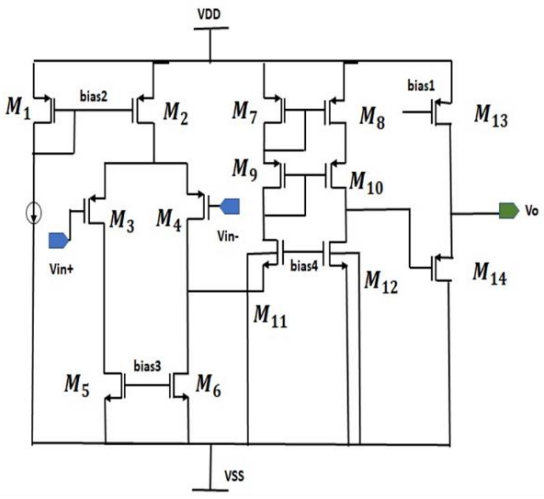
An improved version of INA has been designed with a 0.9V supply as shown in Fig. 9 (a). In this design we have used a traditional 3 stage INA which is designed by employing two folded cascode operational amplifier at two-input stages and at the output stage also, folded cascode operational amplifier which is exhibited in Fig. 9 (b) is utilised. Parameters of the folded cascode amplifier design are provided in Table 1. This design achieved higher gain, higher CMRR and better GBW.

TABLE 1
Folded cascode operational amplifier design parameters

Transistor	Width (W)	Length(L)
$M_1, M_2. M_7, M_8, M_9$	3 µm	1 µm
M_3, M_4	4.45 µm	1 µm
M_5, M_6	4.45 µm	1 µm
M_9, M_{10}	4.45 µm	1 µm
M_{11}, M_{12}	4.45 µm	1 µm



(a)



(b)

Fig. 9. (a) Proposed Instrumentation Amplifier with folded cascode operational amplifier Circuit, (b) Proposed folded cascode operational amplifier circuit

VI. Design Simulations and Results

In this research work, an improved version of the instrumentation amplifier (INA) has been designed utilising a folded cascode operational amplifier with a 0.9 V supply. The value of resistors is set as per Table 2. A proposed instrumentation Amplifier with Folded Cascode topology frequency Response is shown in Fig. 10. A gain of 125.579 dB, CMRR of 147.2556 dB and GBW of 6.179 MHz have been obtained. Table 3 represents the comparative performance of the state of the art.

TABLE 2
Resistance values used in the INA circuit

Resistors (R)	Values
R_1	100 KΩ
R_2	50 Ω
R_3	500 KΩ
R_G	100 KΩ

TABLE 3
Cross-platform comparative performance

Parameter	[16]	[17]	[18]	[19]	[20]	Proposed Work
Technology (µm)	0.35	0.5	0.18	0.18	0.9	0.18
Gain(dB)	33.7	45	67.7	79.16	95.59	125.579
CMRR (dB)	83	75	92	98	108.4	147.2556
Gain Bandwidth (MHz)	2	1.1	1.75	9	3.95	6.179
Power Dissipation (W)	0.85 m	283	263	409.14	4.85 m	25.315µ

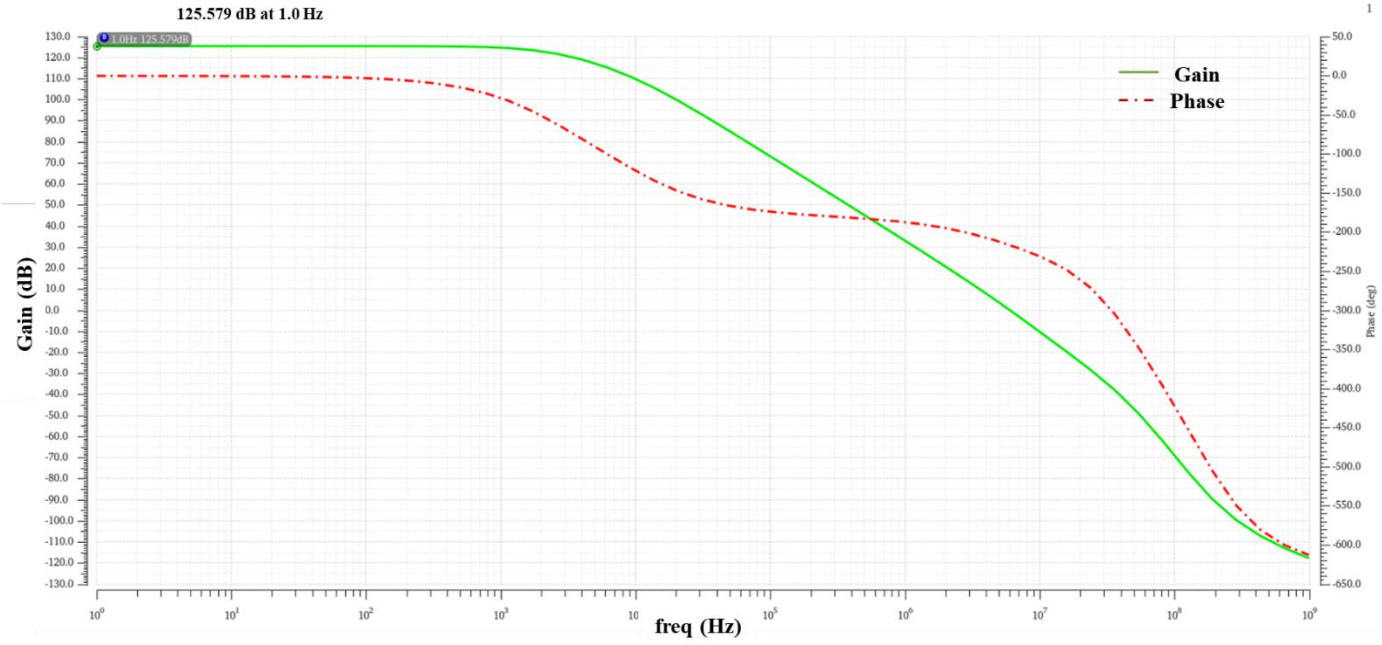


Fig. 10. Gain and Phase response graph of proposed instrumentation amplifier.

VII. CONCLUSION

This paper presents a comprehensive comparative study of various Instrumentation Amplifier (INA) topologies, including local current feedback INA, active CMOS instrumentation amplifier, OP-Amp with folded cascode, modified INA using a differential amplifier, and an area-efficient CMOS INA. Through analysis, it is revealed that the area-efficient CMOS INA achieves superior performance in terms of high gain and CMRR, coupled with a reduced die area, leading to cost savings compared to alternative CMOS instrumentation amplifier designs. The precision of gain and CMRR is further enhanced by employing very high gain Op Amps and increasing the value of differential gains. Specifically, our design featuring a folded cascode operational amplifier attains an impressive 125.579 dB gain, 147.2556 dB CMRR, and 6.179 MHz GBW, outperforming all previously examined designs. These advancements find applications in high-precision measurement systems, Internet of Things (IoT) based systems, medical instrumentation, and other domains requiring accurate signal processing and low-cost solutions.

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